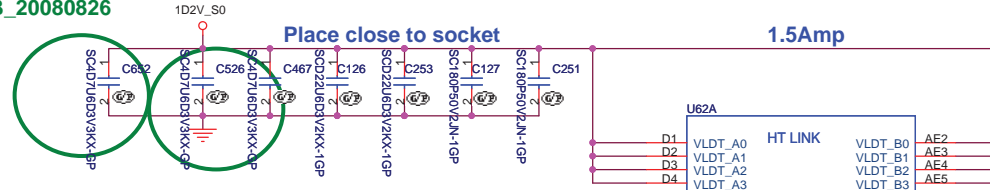
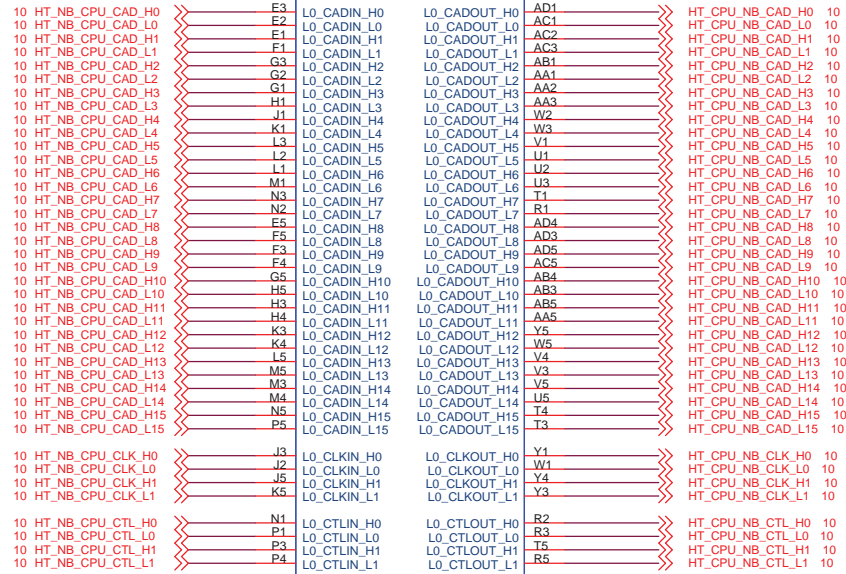


Date: Wednesday, October 01, 2008 Sheet 1 of 47

SB_20080826



SA_20080723

SKT-CPU638P-GP-U2
62.10055.111 2ND = 62.10055.251

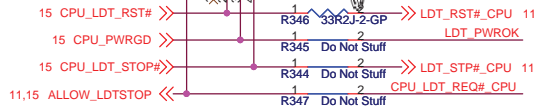
SKT-BGA638H176

| State | Specification | Notes | 2M200100M2303 |
|----------|-----------------|-------|---------------|
| S0.C0.Px | Tcase Max | 3 | TBD |
| | NB COF | 1 | 400 MHz |
| | VID_VDDNB Min | 2 | 0.950 V |
| | VID_VDDNB Max | 2 | 0.950 V |
| | Startup P-state | | S0.C0.P7 |
| | | | |
| S0.C0.P0 | CPU COF | 1 | 2000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | IDD Max | 3 | TBD |
| | | | |
| S0.C0.P1 | CPU COF | 1 | 1800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P2 | CPU COF | 1 | 1500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P3 | CPU COF | 1 | 1300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P4 | CPU COF | 1 | 1000 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P5 | CPU COF | 1 | 800 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P6 | CPU COF | 1 | 500 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |
| S0.C0.P7 | CPU COF | 1 | 300 MHz |
| | TDP | 3 | TBD |
| | VID_VDD Min | 2 | 1.100 V |
| | VID_VDD Max | 2 | 1.125 V |
| | | | |
| | | | |

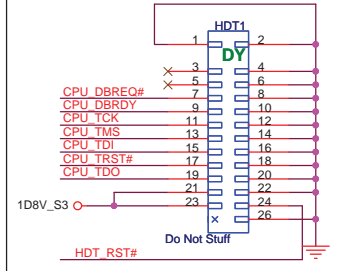
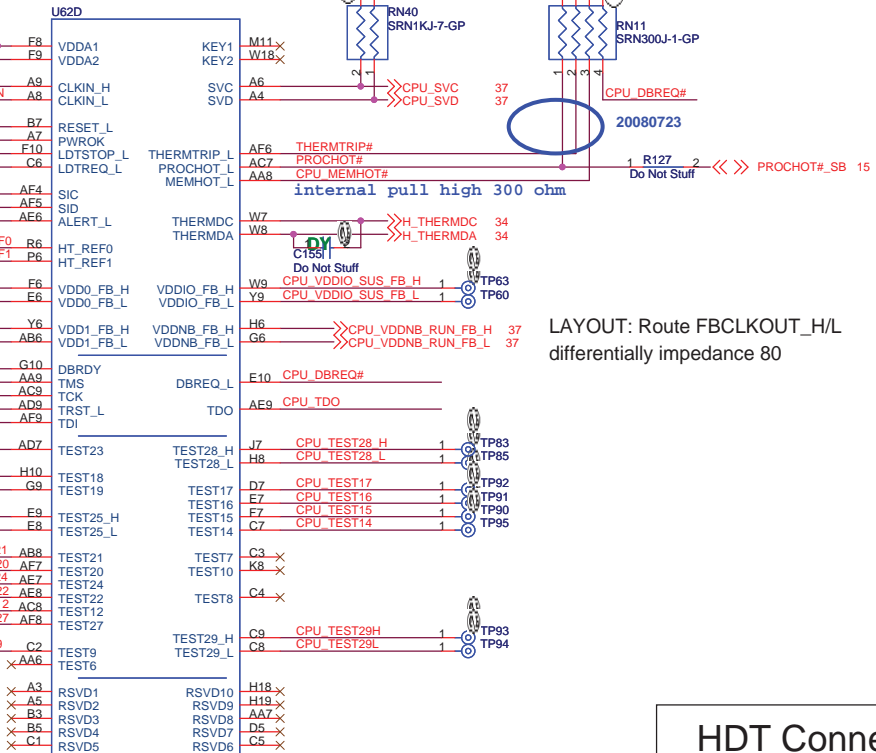
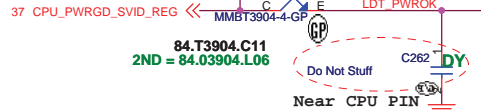
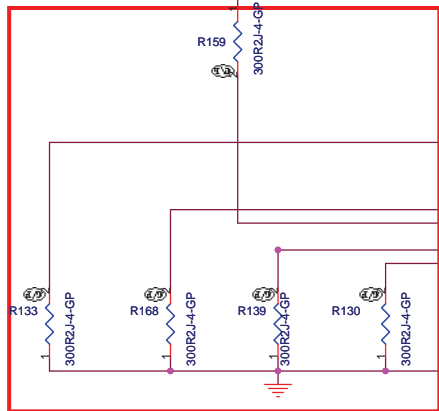
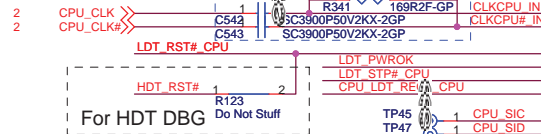
MP

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Taipei Hsien 221, Taiwan, R.O.C.

| | | | | | |
|----------------------------------|-----------------|--|-----------------------|---|-------|
| Title | | | CPU_HT_LINK I/F (1/4) | | |
| Size | Document Number | | | | Rev |
| A3 | F7-GT | | | | -1 |
| Date: Thursday, October 09, 2008 | | | Sheet | 3 | of 47 |



LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.



The Processor has reached a preset maximum operating temperature. 100°C
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L
differentially impedance 80

MP

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Taipei Hsien 221, Taiwan, R.O.C.

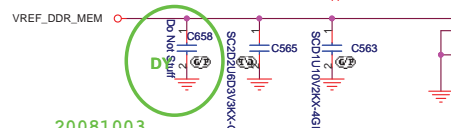
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|------------------------------------|----------------------------|-----------|---------|
| Title | | | |
| CPU_Control&Debug_(3/4) | | | |
| Size | Document Number | Rev | |
| A3 | F7-GT | -1 | |
| Date: | Thursday, October 09, 2008 | Sheet | 5 of 47 |

4.9 MEM_MB_ADD0 >> 102 A0
4.9 MEM_MB_ADD1 >> 101 A1
4.9 MEM_MB_ADD2 >> 100 A2
4.9 MEM_MB_ADD3 >> 99 A3
4.9 MEM_MB_ADD4 >> 98 A4
4.9 MEM_MB_ADD5 >> 97 A5
4.9 MEM_MB_ADD6 >> 96 A6
4.9 MEM_MB_ADD7 >> 95 A7
4.9 MEM_MB_ADD8 >> 94 A8
4.9 MEM_MB_ADD9 >> 93 A9
4.9 MEM_MB_ADD10 >> 105 A10/AP
4.9 MEM_MB_ADD11 >> 90 A11
4.9 MEM_MB_ADD12 >> 89 A12
4.9 MEM_MB_ADD13 >> 116 A13
4.9 MEM_MB_ADD14 >> 86 A14
4.9 MEM_MB_ADD15 >> 84 A15
4.9 MEM_MB_BANK2 >> 107 BA0
4.9 MEM_MB_BANK0 >> 106 BA1
4.9 MEM_MB_BANK1 >> 106 BA1

4 MEM_MB_DATA0 >> 5 DQ0
4 MEM_MB_DATA1 >> 17 DQ1
4 MEM_MB_DATA2 >> 19 DQ2
4 MEM_MB_DATA3 >> 18 DQ3
4 MEM_MB_DATA4 >> 4 DQ4
4 MEM_MB_DATA5 >> 6 DQ5
4 MEM_MB_DATA6 >> 14 DQ6
4 MEM_MB_DATA7 >> 14 DQ7
4 MEM_MB_DATA8 >> 23 DQ8
4 MEM_MB_DATA9 >> 35 DQ9
4 MEM_MB_DATA10 >> 37 DQ10
4 MEM_MB_DATA11 >> 20 DQ11
4 MEM_MB_DATA12 >> 22 DQ12
4 MEM_MB_DATA13 >> 36 DQ13
4 MEM_MB_DATA14 >> 38 DQ14
4 MEM_MB_DATA15 >> 43 DQ15
4 MEM_MB_DATA16 >> 43 DQ16
4 MEM_MB_DATA17 >> 45 DQ17
4 MEM_MB_DATA18 >> 55 DQ18
4 MEM_MB_DATA19 >> 57 DQ19
4 MEM_MB_DATA20 >> 44 DQ20
4 MEM_MB_DATA21 >> 46 DQ21
4 MEM_MB_DATA22 >> 58 DQ22
4 MEM_MB_DATA23 >> 58 DQ23
4 MEM_MB_DATA24 >> 61 DQ24
4 MEM_MB_DATA25 >> 63 DQ25
4 MEM_MB_DATA26 >> 73 DQ26
4 MEM_MB_DATA27 >> 75 DQ27
4 MEM_MB_DATA28 >> 62 DQ28
4 MEM_MB_DATA29 >> 64 DQ29
4 MEM_MB_DATA30 >> 76 DQ30
4 MEM_MB_DATA31 >> 123 DQ31
4 MEM_MB_DATA32 >> 125 DQ32
4 MEM_MB_DATA33 >> 125 DQ33
4 MEM_MB_DATA34 >> 135 DQ34
4 MEM_MB_DATA35 >> 137 DQ35
4 MEM_MB_DATA36 >> 124 DQ36
4 MEM_MB_DATA37 >> 126 DQ37
4 MEM_MB_DATA38 >> 134 DQ38
4 MEM_MB_DATA39 >> 136 DQ39
4 MEM_MB_DATA40 >> 141 DQ40
4 MEM_MB_DATA41 >> 143 DQ41
4 MEM_MB_DATA42 >> 151 DQ42
4 MEM_MB_DATA43 >> 153 DQ43
4 MEM_MB_DATA44 >> 140 DQ44
4 MEM_MB_DATA45 >> 142 DQ45
4 MEM_MB_DATA46 >> 152 DQ46
4 MEM_MB_DATA47 >> 154 DQ47
4 MEM_MB_DATA48 >> 157 DQ48
4 MEM_MB_DATA49 >> 159 DQ49
4 MEM_MB_DATA50 >> 173 DQ50
4 MEM_MB_DATA51 >> 175 DQ51
4 MEM_MB_DATA52 >> 158 DQ52
4 MEM_MB_DATA53 >> 160 DQ53
4 MEM_MB_DATA54 >> 174 DQ54
4 MEM_MB_DATA55 >> 176 DQ55
4 MEM_MB_DATA56 >> 179 DQ56
4 MEM_MB_DATA57 >> 181 DQ57
4 MEM_MB_DATA58 >> 189 DQ58
4 MEM_MB_DATA59 >> 191 DQ59
4 MEM_MB_DATA60 >> 180 DQ60
4 MEM_MB_DATA61 >> 182 DQ61
4 MEM_MB_DATA62 >> 192 DQ62
4 MEM_MB_DATA63 >> 194 DQ63

4 MEM_MB_DQS0_N >> 29 DQS0#
4 MEM_MB_DQS1_N >> 49 DQS1#
4 MEM_MB_DQS2_N >> 68 DQS2#
4 MEM_MB_DQS3_N >> 129 DQS3#
4 MEM_MB_DQS4_N >> 146 DQS4#
4 MEM_MB_DQS5_N >> 167 DQS5#
4 MEM_MB_DQS6_N >> 186 DQS6#
4 MEM_MB_DQS7_N >> 186 DQS7#
4 MEM_MB_DQS0_P >> 13 DQS0
4 MEM_MB_DQS1_P >> 31 DQS1
4 MEM_MB_DQS2_P >> 51 DQS2
4 MEM_MB_DQS3_P >> 70 DQS3
4 MEM_MB_DQS4_P >> 131 DQS4
4 MEM_MB_DQS5_P >> 148 DQS5
4 MEM_MB_DQS6_P >> 169 DQS6
4 MEM_MB_DQS7_P >> 188 DQS7

4.9 MEM_MB_ODT0 >> 114
4.9 MEM_MB_ODT1 >> 119



20081003

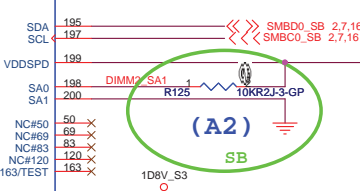
Place C2.2uF and 0.1uF < 500mils from DDR connector

REVERSE TYPE

62.10017.661

2ND = 62.10017.A41
LOW 5.2 mm

RAS# 108 >> MEM_MB_RAS# 4.9
WE# 109 >> MEM_MB_WE# 4.9
CAS# 113 >> MEM_MB_CAS# 4.9
CS0# 110 >> MEM_MB_CS0 4.9
CS1# 115 >> MEM_MB_CS1 4.9
CKE0 79 >> MEM_MB_CKE0 4.9
CKE1 80 >> MEM_MB_CKE1 4.9
CK0 30 >> MEM_MB_CLK0_P 4
CK0# 32 >> MEM_MB_CLK0_N 4
CK1 164 >> MEM_MB_CLK1_P 4
CK1# 166 >> MEM_MB_CLK1_N 4
DM0 10 >> MEM_MB_DM0 4
DM1 26 >> MEM_MB_DM1 4
DM2 52 >> MEM_MB_DM2 4
DM3 67 >> MEM_MB_DM3 4
DM4 130 >> MEM_MB_DM4 4
DM5 147 >> MEM_MB_DM5 4
DM6 170 >> MEM_MB_DM6 4
DM7 185 >> MEM_MB_DM7 4



VDDSPD 199
SA0 198
SA1 200
NC#50 50
NC#69 69
NC#83 83
CH120 120
NC#163/TEST 163

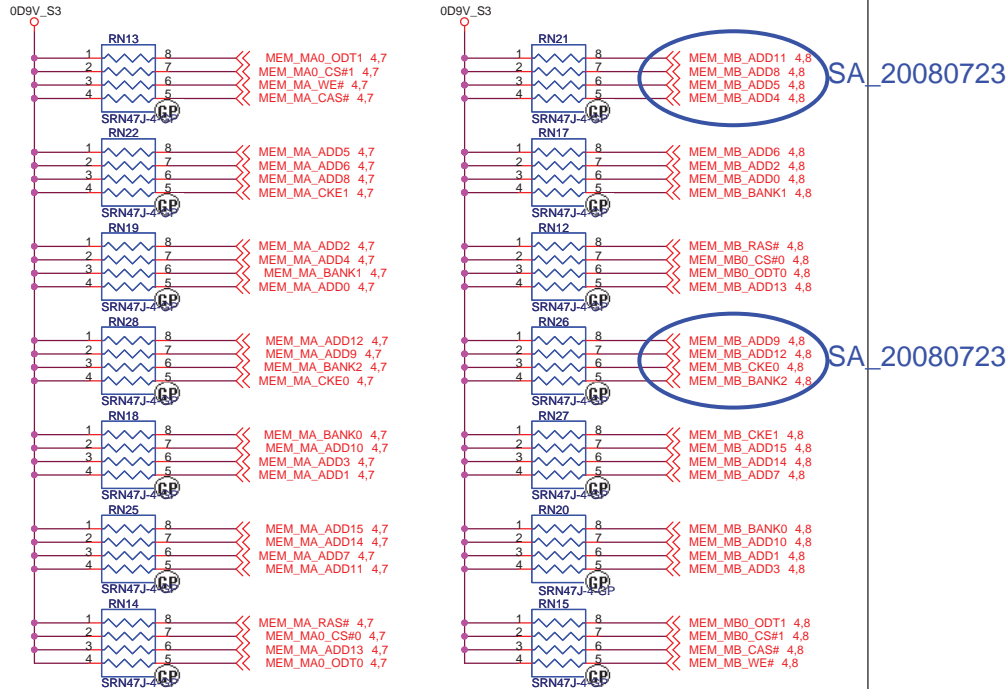
VDD 81
VDD 82
VDD 87
VDD 88
VDD 89
VDD 96
VDD 103
VDD 104
VDD 111
VDD 112
VDD 122
VDD 117
VDD 118
VSS 3
VSS 8
VSS 9
VSS 12
VSS 15
VSS 18
VSS 21
VSS 27
VSS 28
VSS 33
VSS 34
VSS 39
VSS 40
VSS 41
VSS 42
VSS 47
VSS 48
VSS 49
VSS 53
VSS 54
VSS 59
VSS 60
VSS 65
VSS 66
VSS 71
VSS 72
VSS 77
VSS 78
VSS 121
VSS 122
VSS 127
VSS 128
VSS 132
VSS 133
VSS 138
VSS 139
VSS 144
VSS 145
VSS 149
VSS 150
VSS 155
VSS 156
VSS 161
VSS 162
VSS 165
VSS 168
VSS 171
VSS 172
VSS 177
VSS 178
VSS 183
VSS 184
VSS 187
VSS 190
VSS 193
VSS 196
GND 201

GND 201
MH2 201
MH1 202



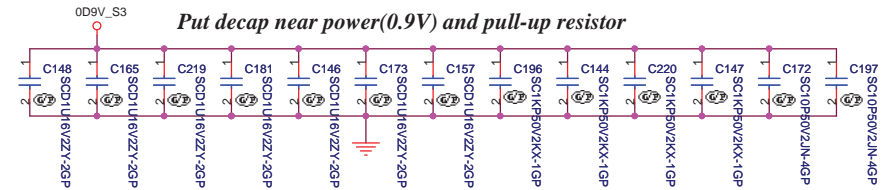
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

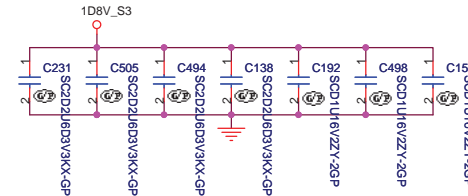


Do not share the Term resistor between the DDR address and Control Signals.

Decoupling Capacitor

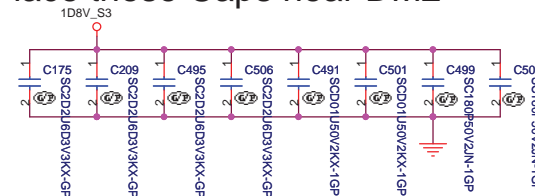


Place these Caps near DM1

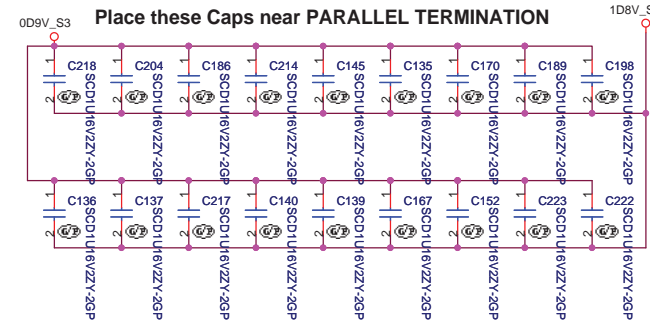


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3

Place these Caps near DM2



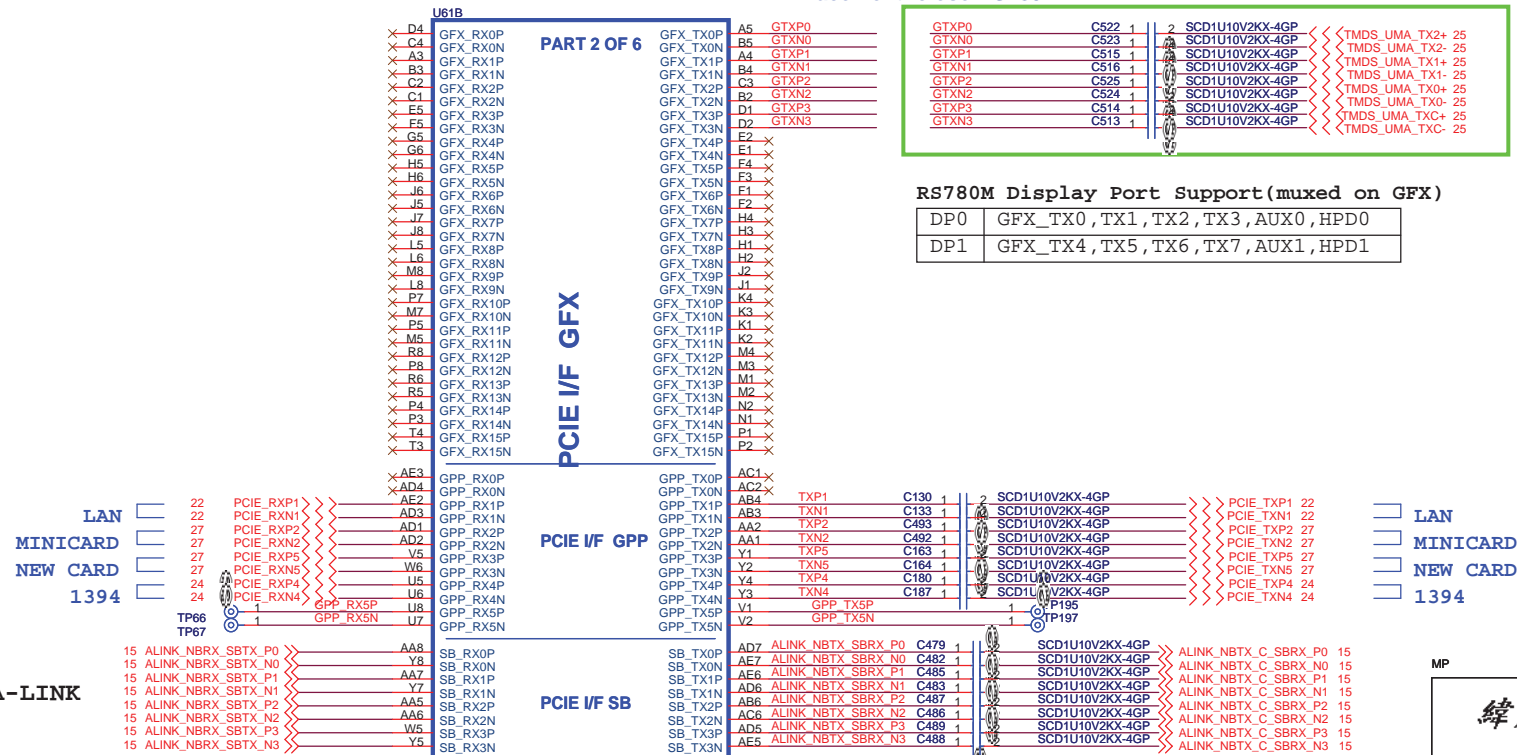
Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0.9V_S3



MP

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| Title | | |
|----------------------------------|-----------------------|--------|
| DDR DAMPING & TERMINATION | | |
| Size A3 | Document Number F7-GT | Rev -1 |
| Date: Thursday, October 09, 2008 | Sheet 9 | of 47 |



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ATI-RS780M_HT LINK&PCIE(1/3)

F7-GT

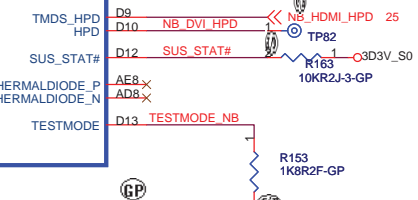
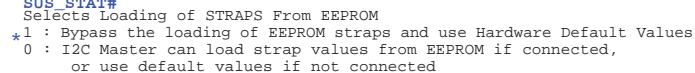
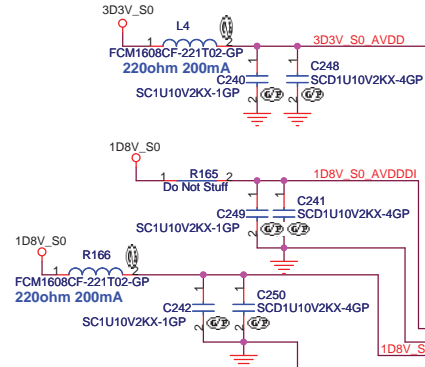
Rev -1

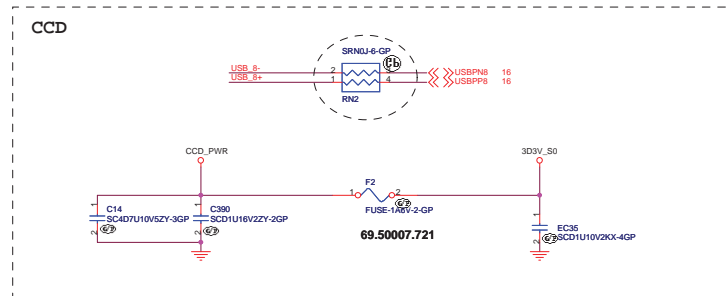
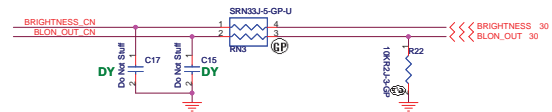
Size A3

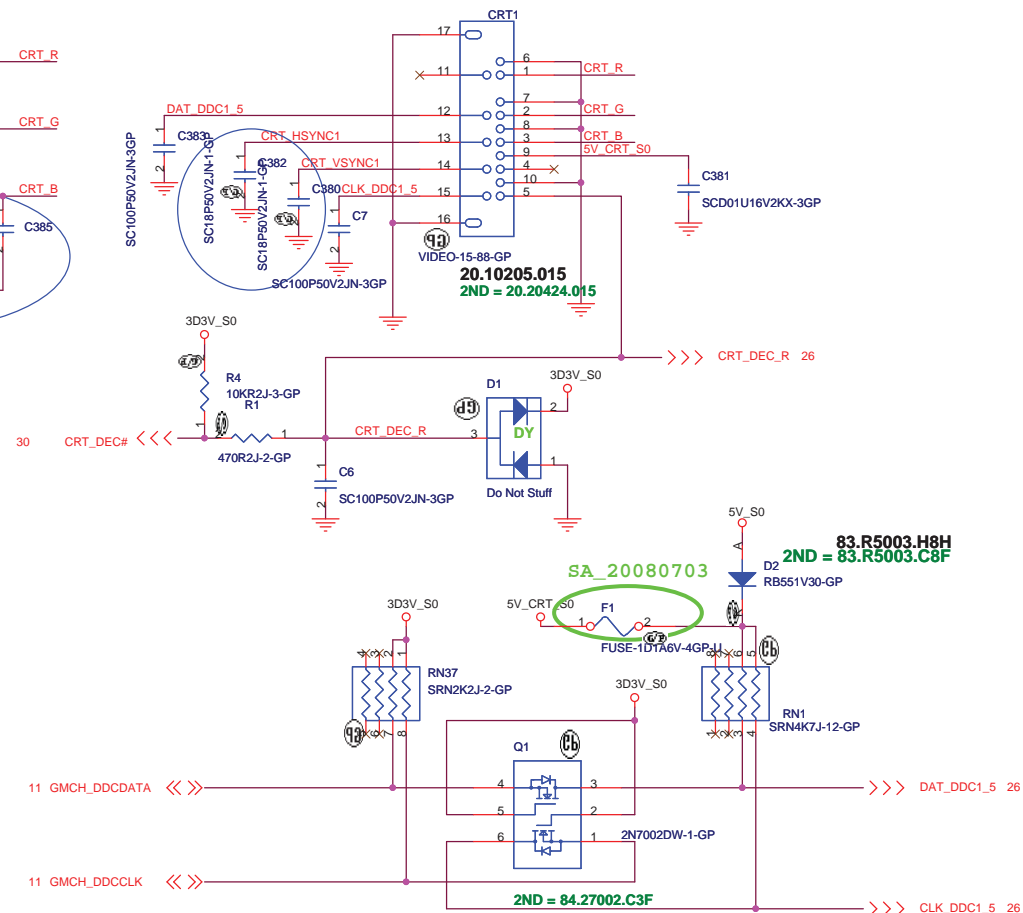
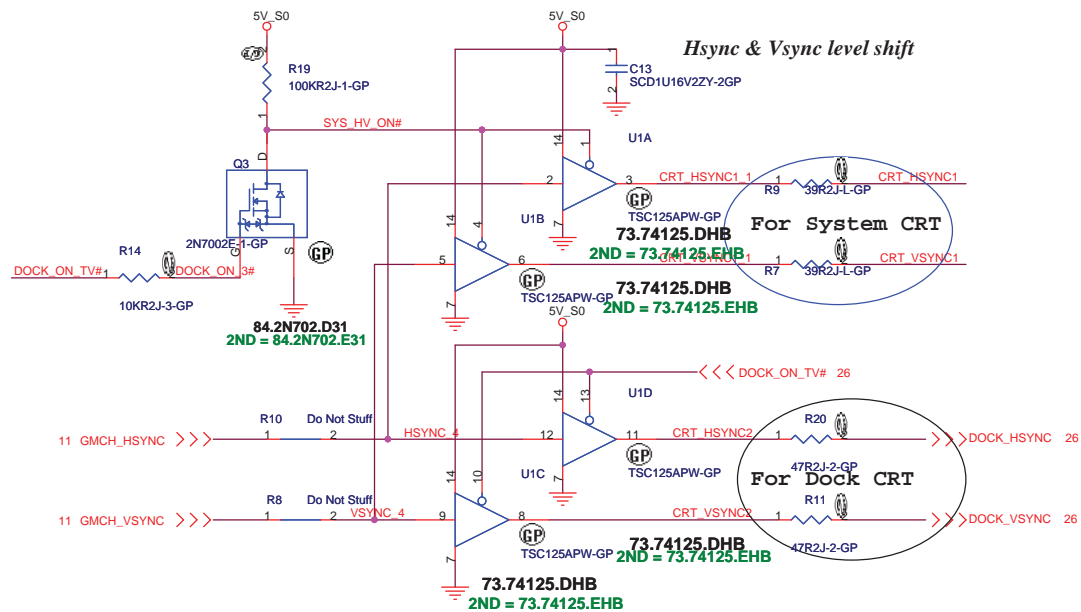
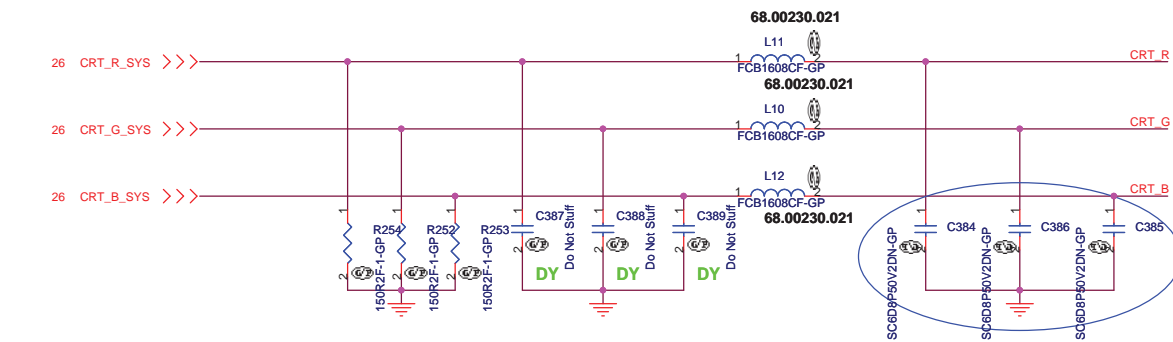
Document Number

Date: Thursday, October 09, 2008

Sheet 10 of 47



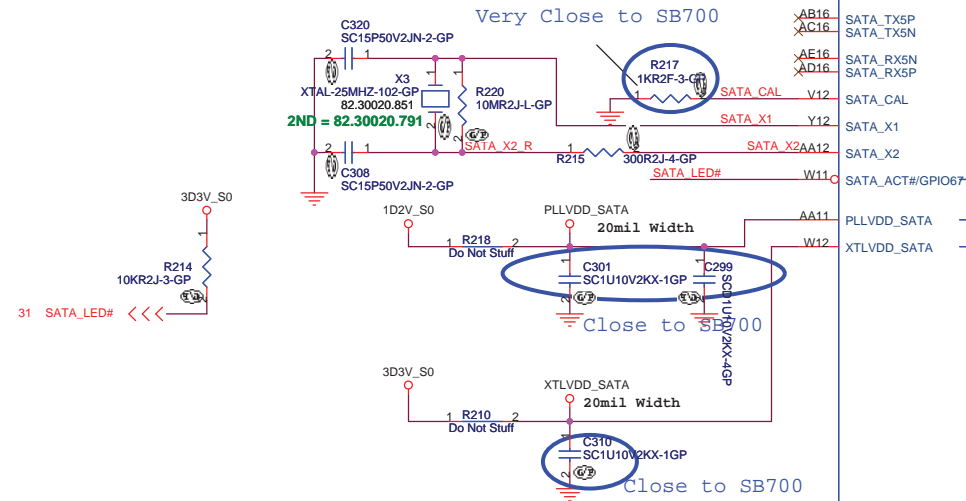
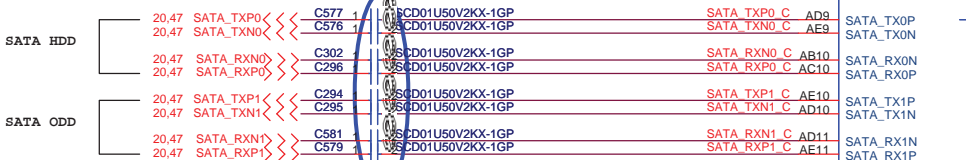




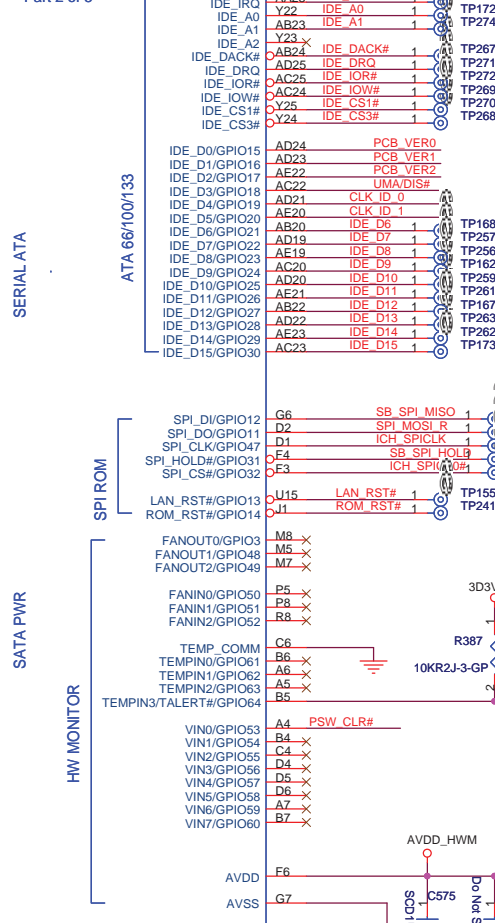




PLACE SATA AC DECOUPLING
CAPS CLOSE TO SB700

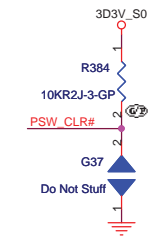
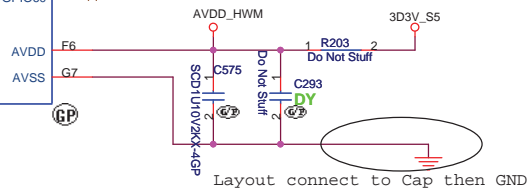
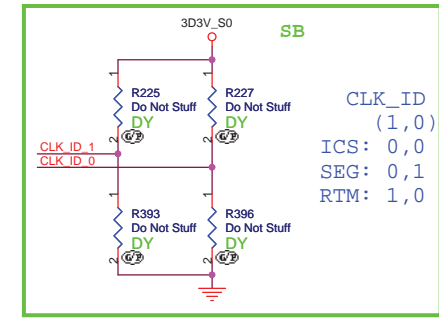
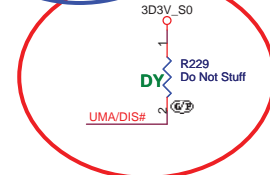
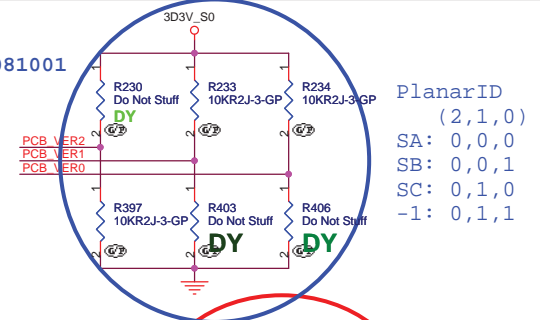


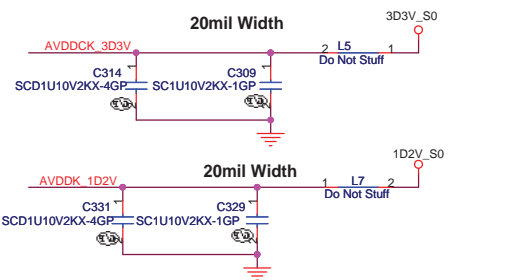
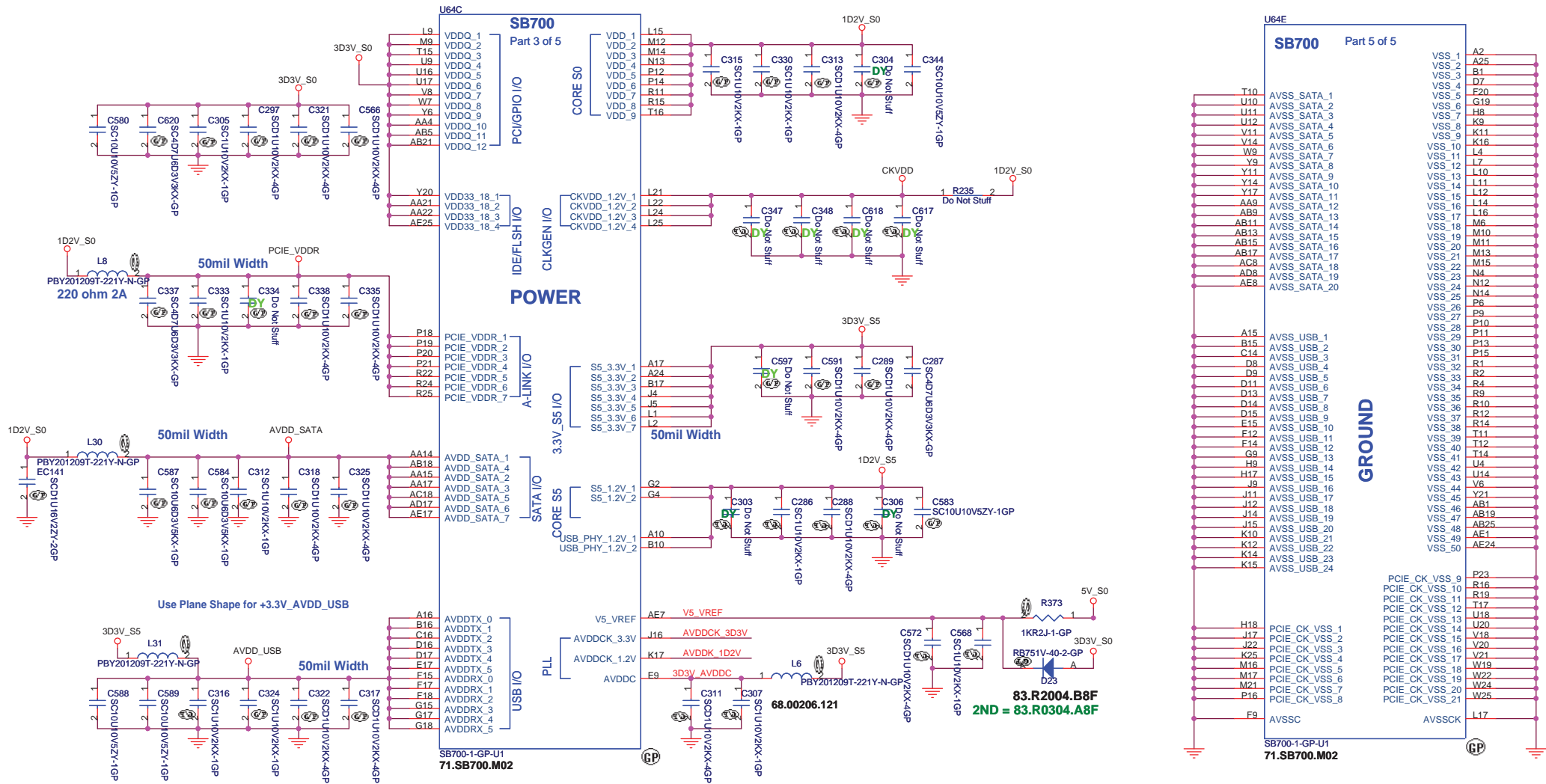
SB700 Part 2 of 5



SB700-1-GP-U1
71.SB700.M02

-1_20081001



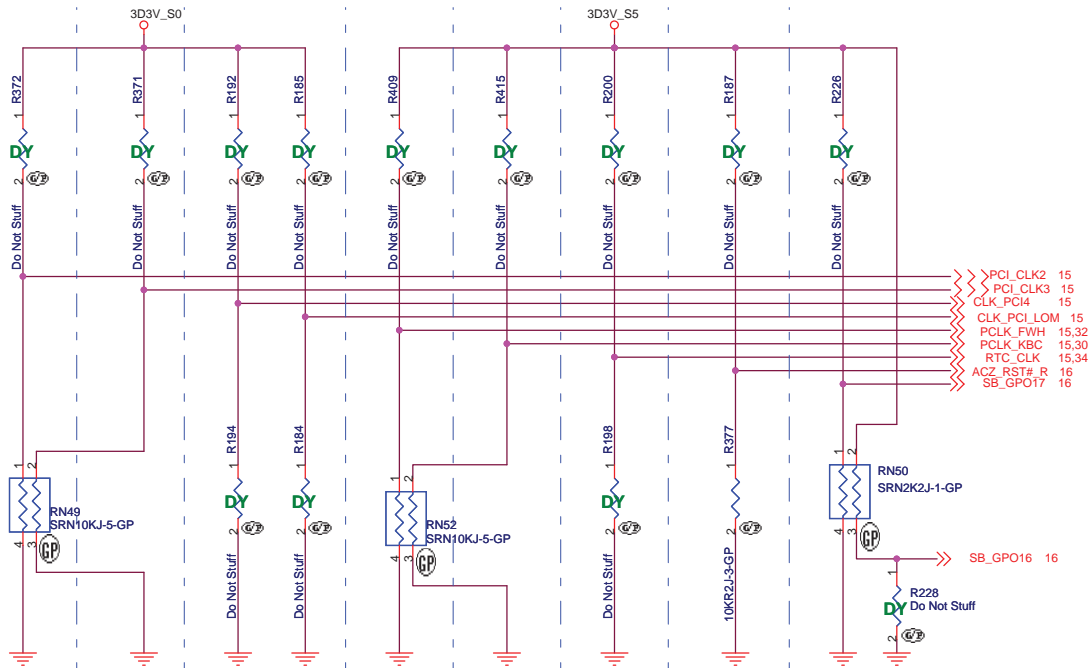


MP

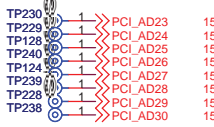
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21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title **ATi-SB700 POWER&GND (4/5)**
Size **A3** Document Number **F7-GT** Rev **-1**
Date: Wednesday, October 01, 2008 Sheet 18 of 47

REQUIRED STRAPS
REQUIRED SYSTEM STRAPS



DEBUG STRAPS



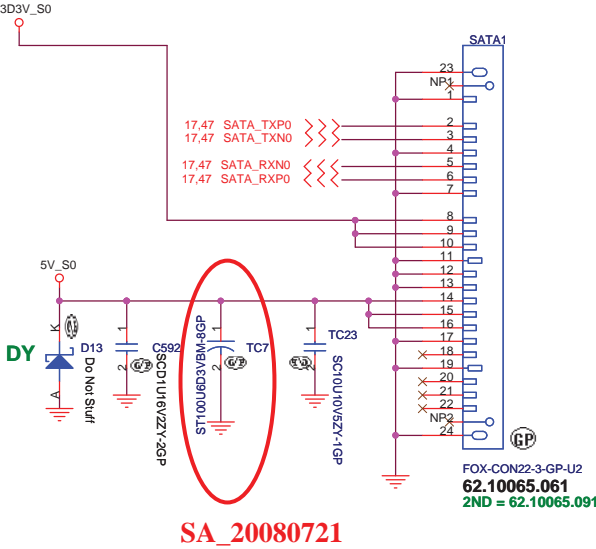
| | PCI_CLK2 | PCI_CLK3 | CLK_PCI_LOM CLK_PCI4 | PCLK_FWH | PCLK_KBC | RTCCLK | AZ_RST# | SB_GPO17 , SB_GPO16 |
|-----------|---|--------------------------------------|-------------------------|----------------------------|---|---|------------------------------------|---|
| PULL HIGH | WatchDOG (NB_PWRGD) ENABLED | USE DEBUG STRAPS | RESERVED | IMC ENABLED | CLKGEN ENABLED (Use Internal) | INTERNAL RTC DEFAULT | ENABLE PCI ROM BOOT | ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT |
| PULL LOW | WatchDog (NB_PWRGD) DISABLED DEFAULT | IGNORE DEBUG STRAPS DEFAULT | | IMC DISABLED DEFAULT | CLKGEN DISABLED (Use External) DEFAULT | EXT. RTC (PD on X1, apply 32KHz to RTC_CLK) | DISABLE PCI ROM BOOT DEFAULT | L, H = LPC ROM L, L = FWH ROM |

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

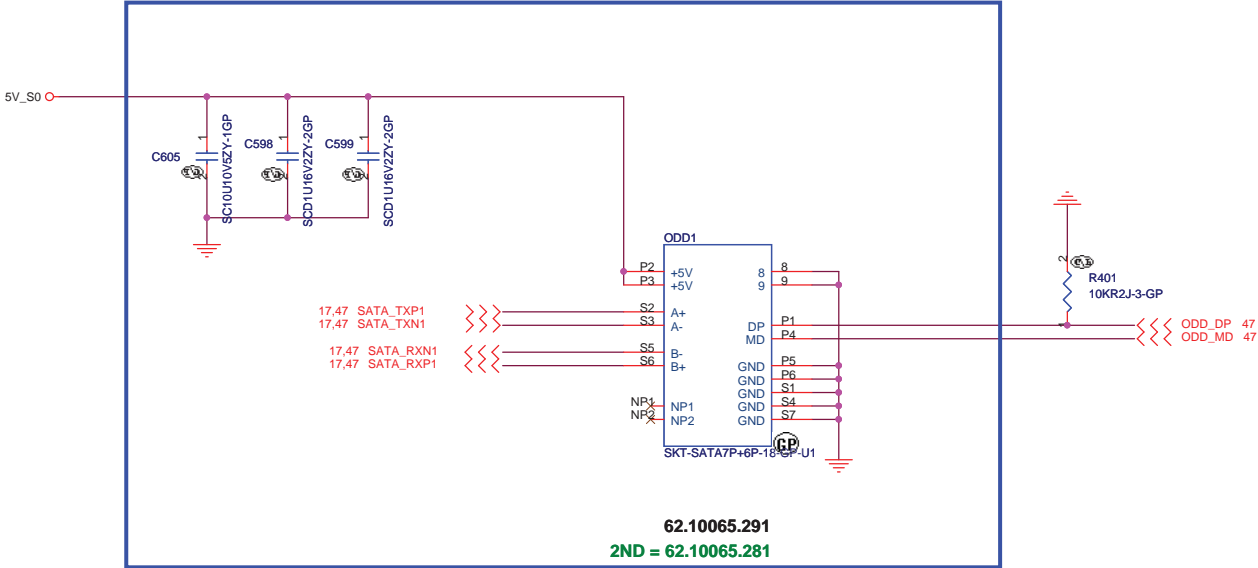
| | PCI_AD28 | PCI_AD27 | PCI_AD26 | PCI_AD25 | PCI_AD24 | PCI_AD23 | PCI_AD30 PCI_AD29 |
|-----------|-----------------------------------|-----------------------------|-------------------------------|-----------------------------|---|-----------------------|----------------------|
| PULL HIGH | USE LONG RESET (DEFAULT) | USE PCI PLL (DEFAULT) | USE ACPI BCLK (DEFAULT) | USE IDE PLL (DEFAULT) | USE DEFAULT PCIE STRAPS (DEFAULT) | Reserved (DEFAULT) | Reserved |
| PULL LOW | USE SHORT RESET | BYPASS PCI PLL | BYPASS ACPI BCLK | BYPASS IDE PLL | USE EEPROM PCIE STRAPS | Reserved | |

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

SATA HDD Connector



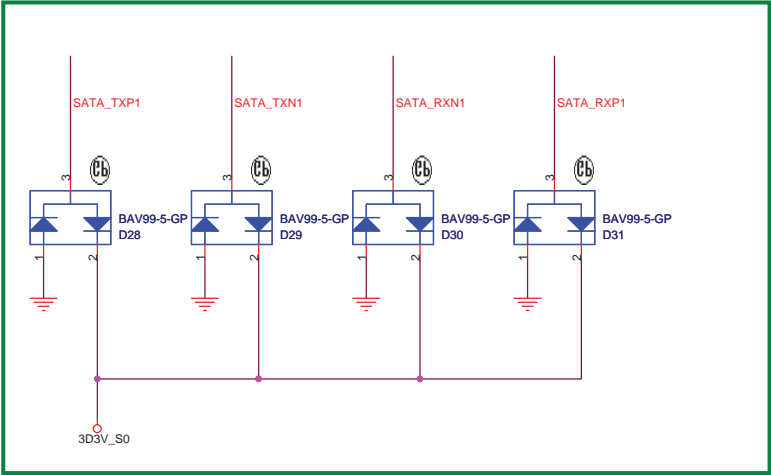
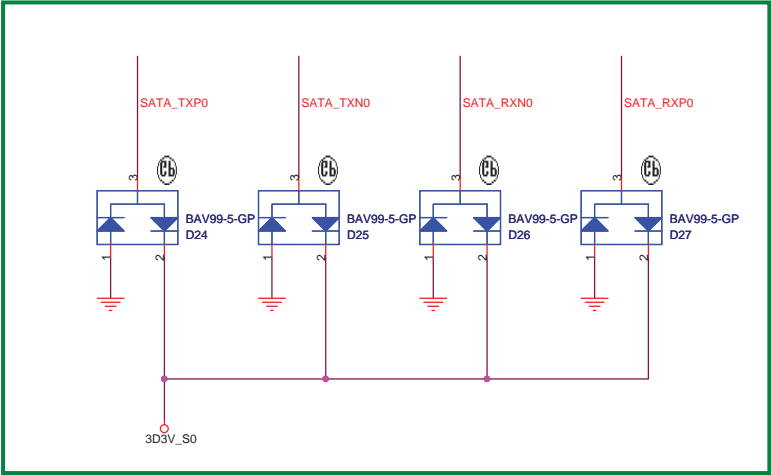
SA_20080714 SATA ODD Connector

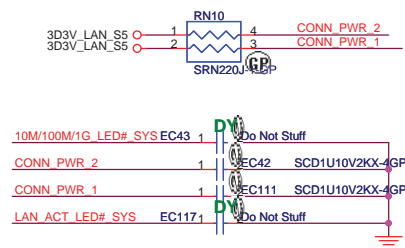


For HDD

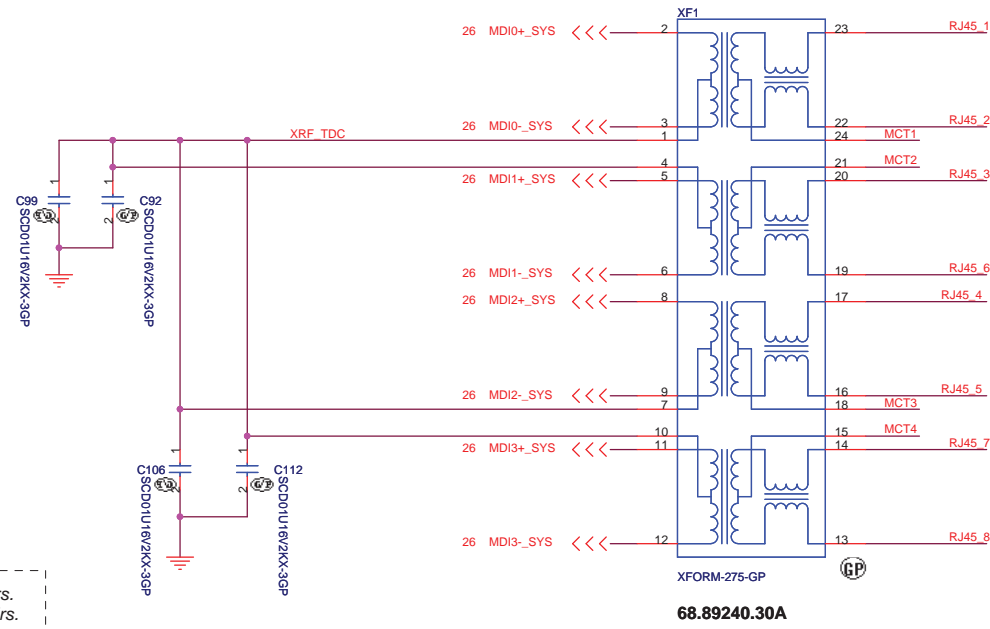
SB_20080825

For ODD



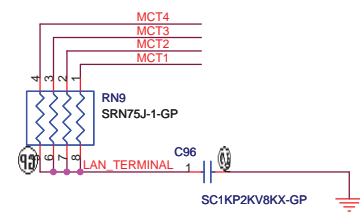


GIGA Lan Transformer

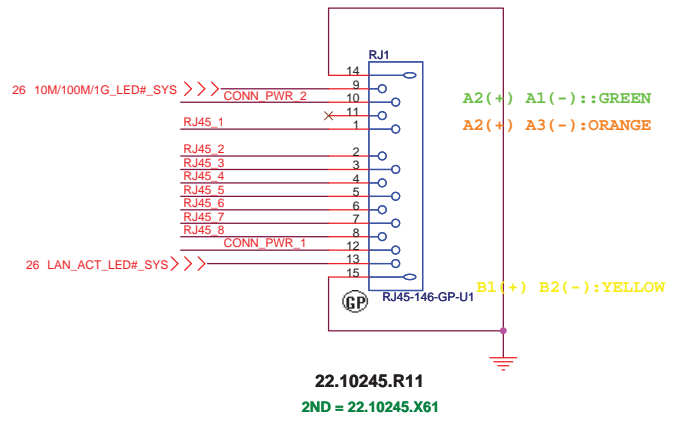


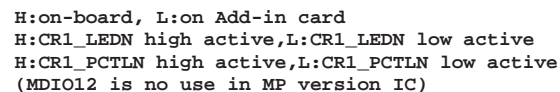
- 1.route on bottom as differential pairs.
- 2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
- 3.No vias, No 90 degree bends.
- 4.pairs must be equal lengths.
- 5.6mil trace width, 12mil separation.
- 6.36mil between pairs and any other trace.
- 7.Must not cross ground moat, except RJ-45 moat.

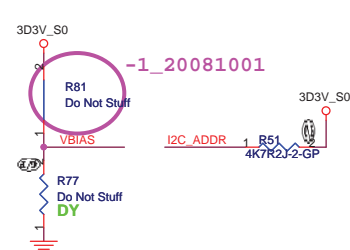
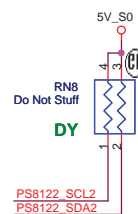
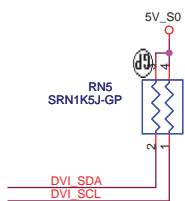
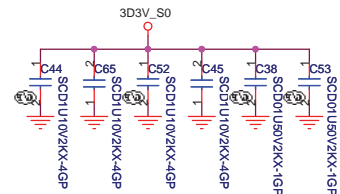
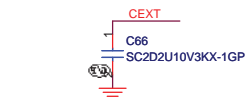
| 10/100 LAN Transformer | RJ45 PIN |
|------------------------|----------|
| TD+ --> TX+ | RJ45-1 |
| TD- --> TX- | RJ45-2 |
| RD+ --> RX+ | RJ45-3 |
| RD- --> RX- | RJ45-6 |



LAN Connector

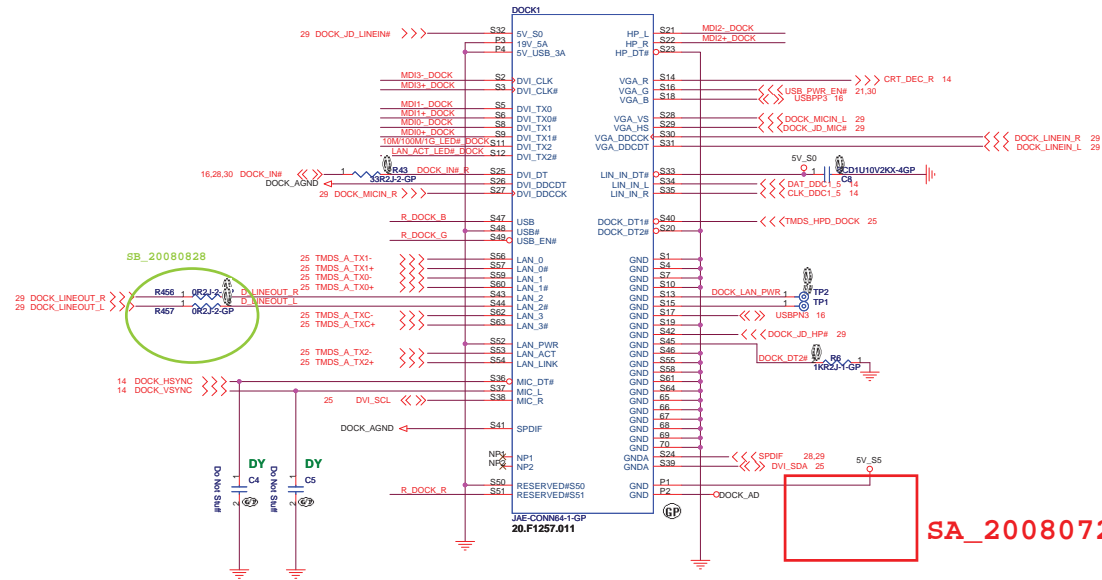




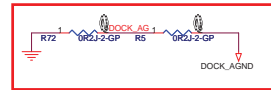


SA_20080709 change to Port Replicator

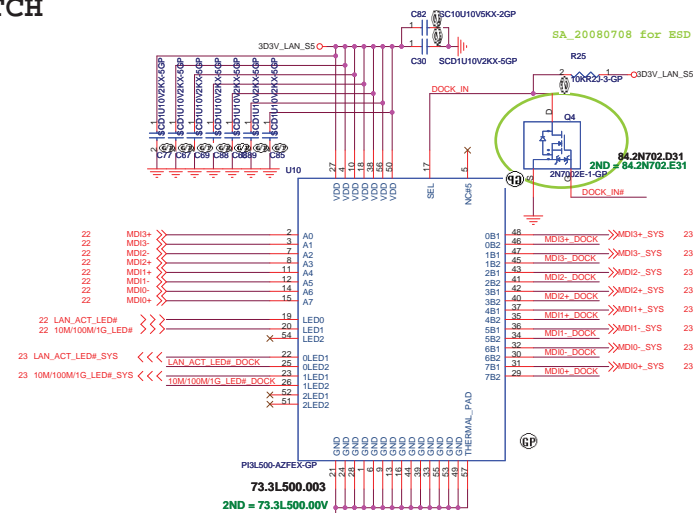
DOCK



SA_20080724

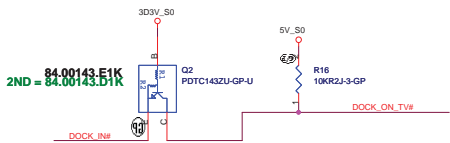


LAN SWITCH

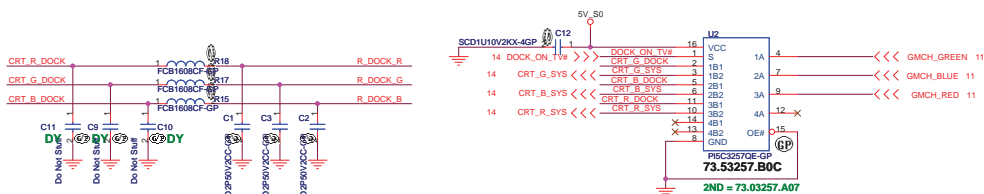


| Function | LAN |
|----------|-----|
| SYSTEM | L |
| DOCK | H |

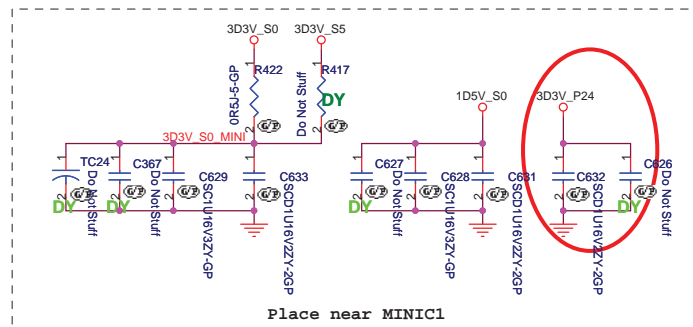
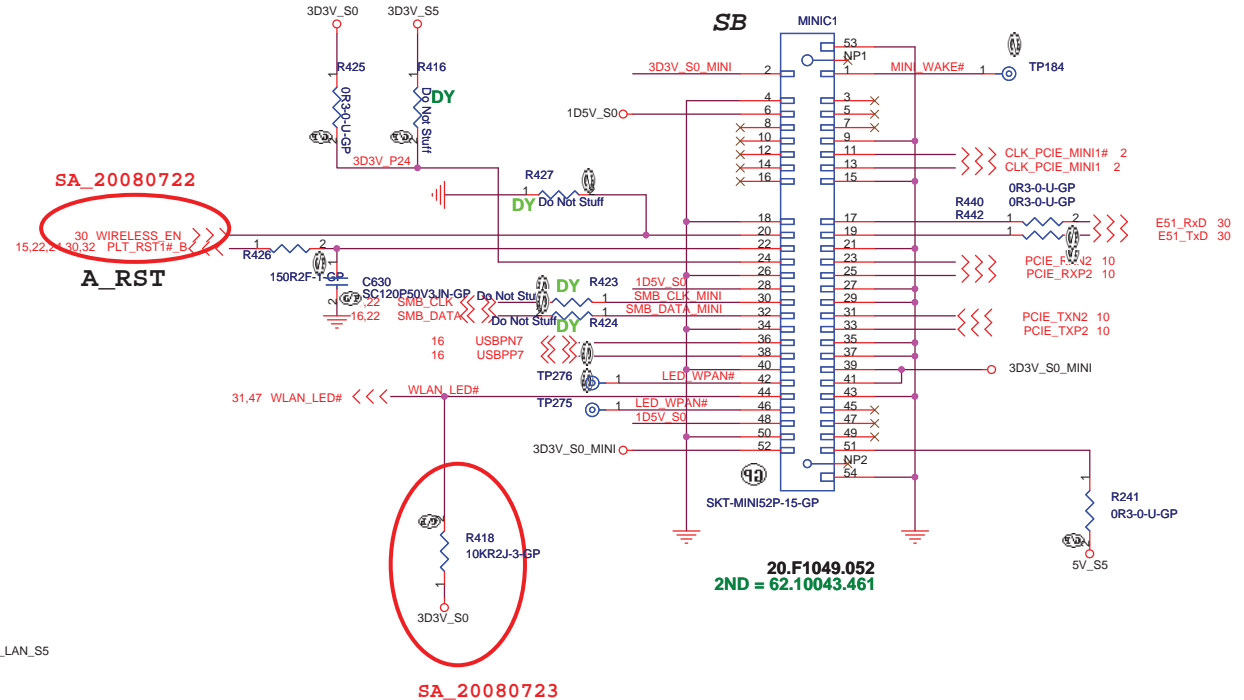
CRT SWITCH

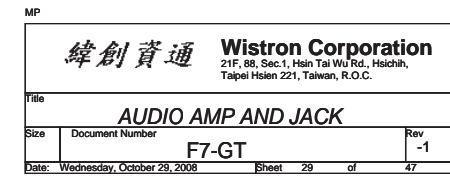
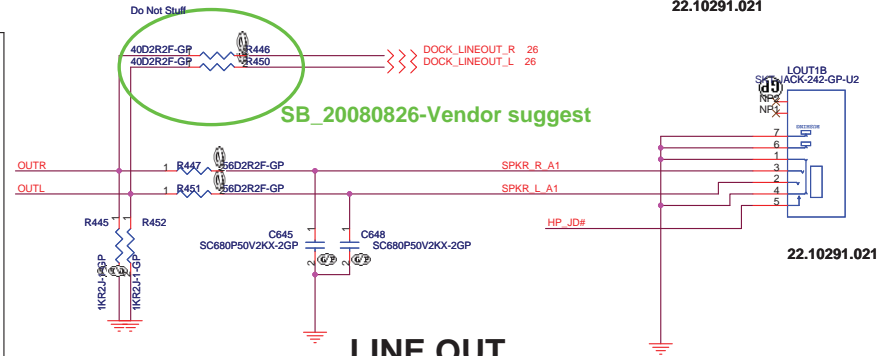
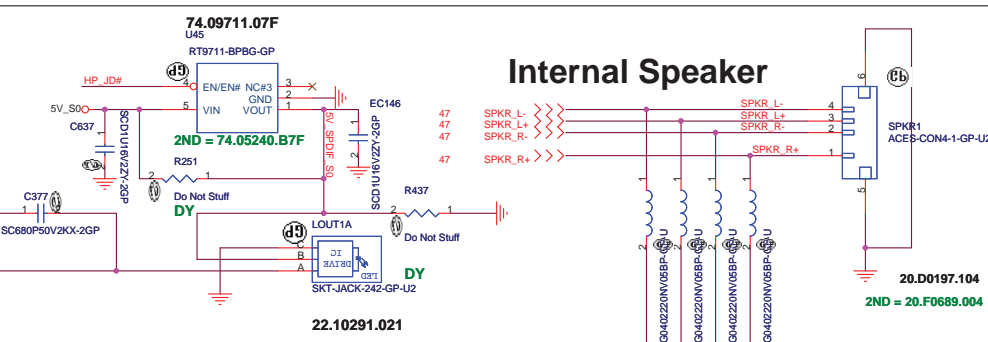
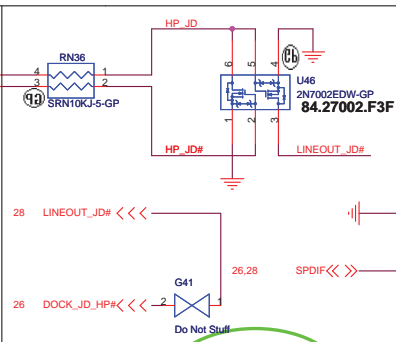
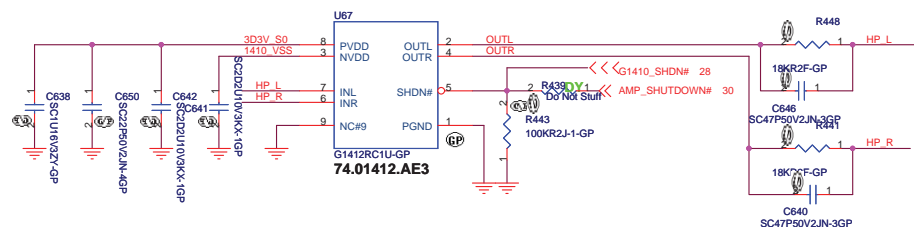
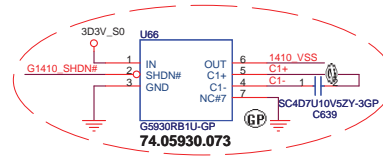


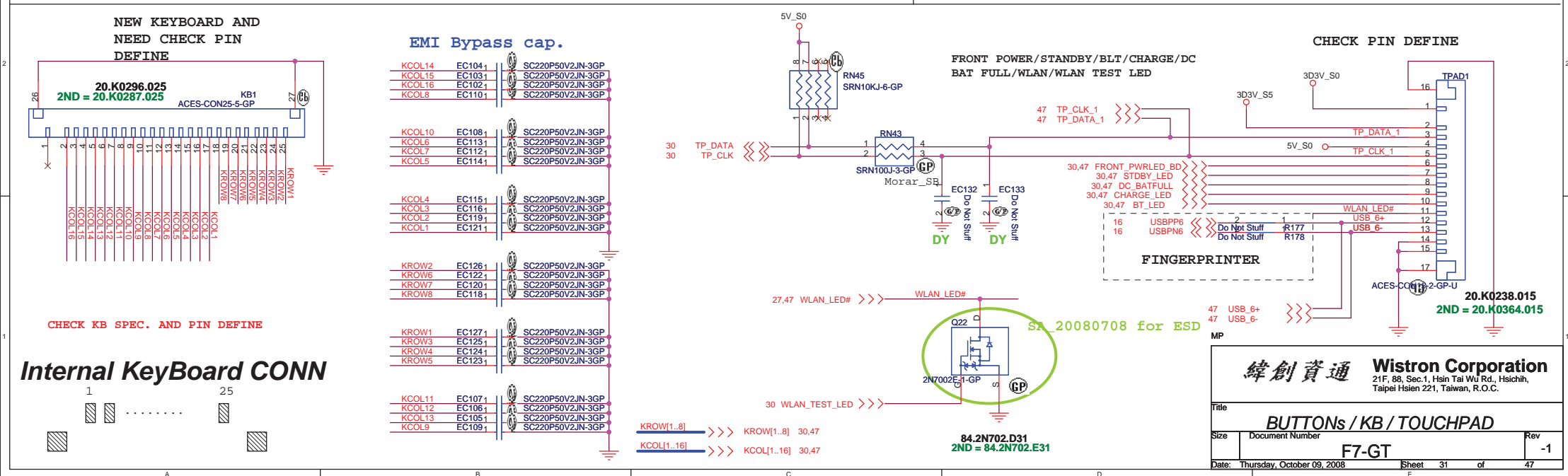
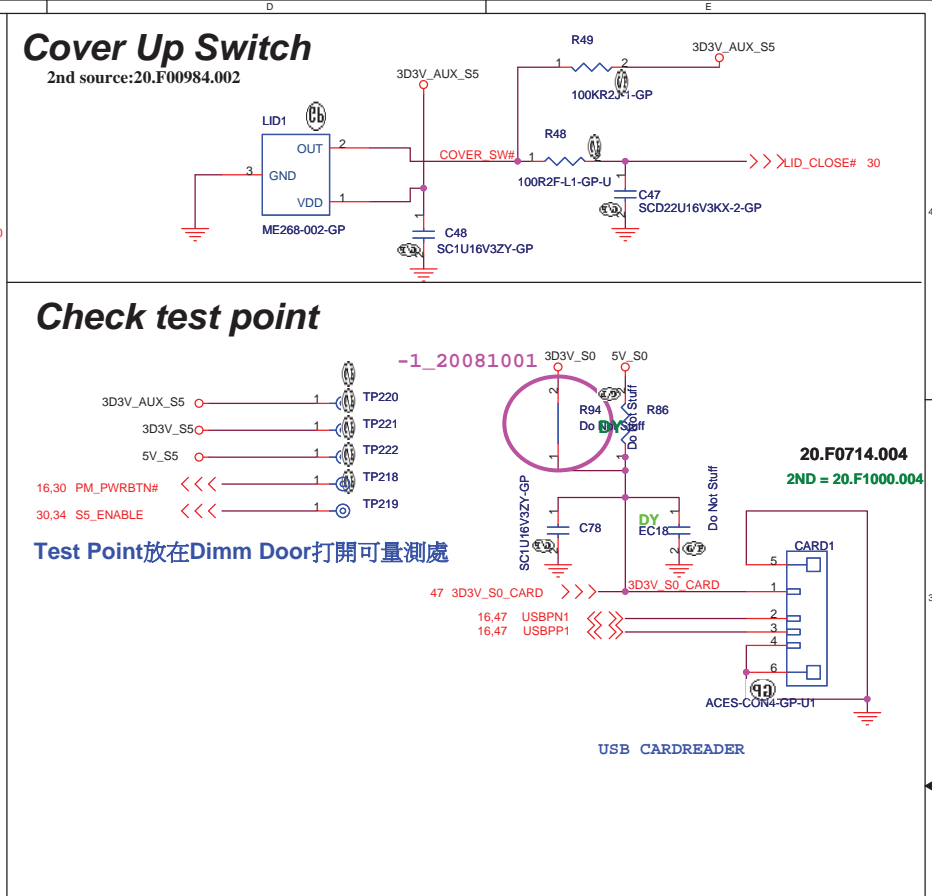
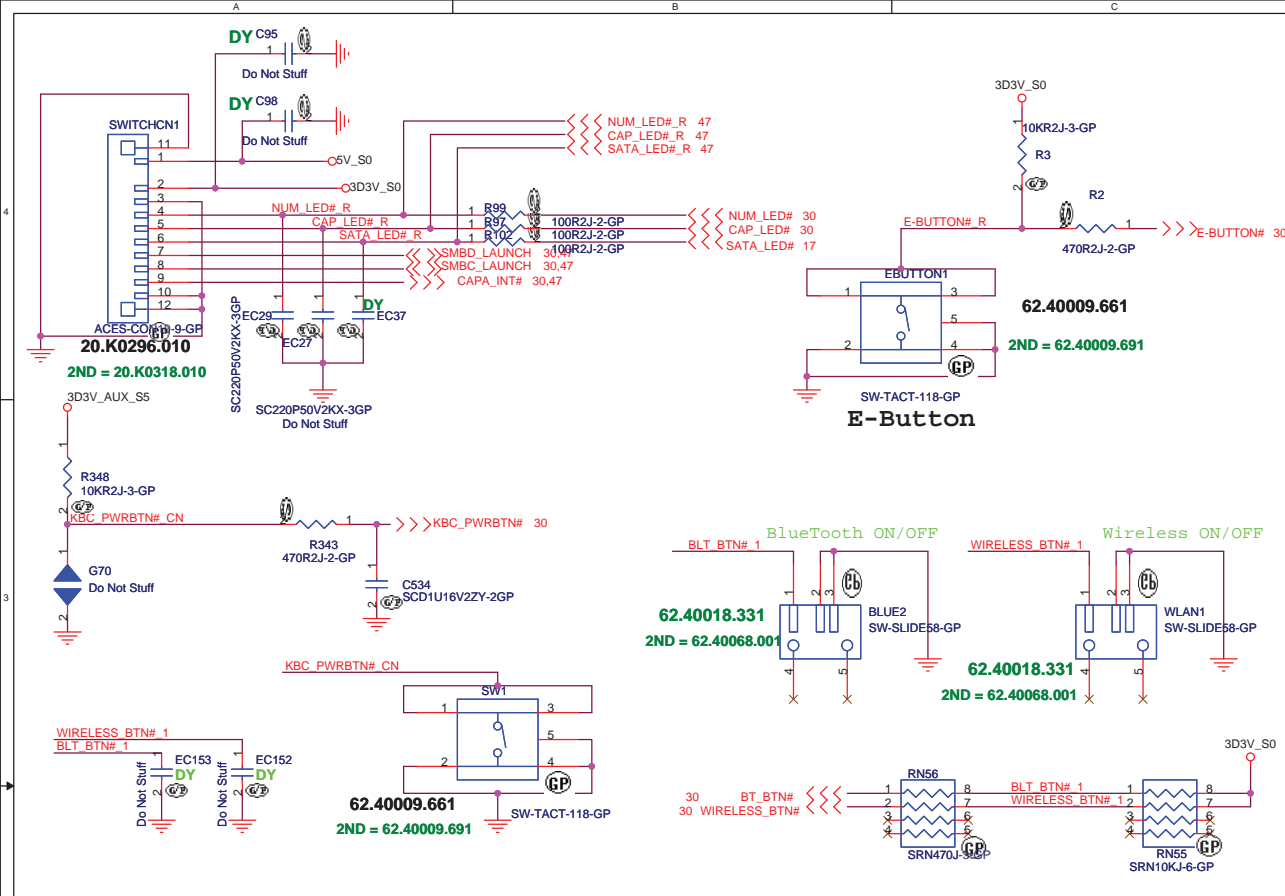
| Function | CRT | TV |
|----------|-----|----|
| SYSTEM | H | H |
| DOCK | L | L |



Mini Card Connector







16M Bits



| | |
|----------|----------|
| A15 | (B1) |
| A14 | (B2) |
| \vdots | \vdots |
| A2 | (B14) |
| A1 | (B15) |

The diagram illustrates the connection of the SA_20080722 component to the U39 chip. The component is connected to the chip's pins A1 through A15 and B1 through B15. The connections are as follows:

- Power and Ground:**
 - 5V_S0 is connected to A1 and B1.
 - 3D3V_S0 is connected to A7 and B7.
 - 3D3V_S0 is connected to A15 and B15.
- Signal Connections:**
 - A2 is connected to B1 (PLT_RST1#_B).
 - A3 is connected to B2 (LPC_LFRAME#).
 - A4 is connected to B3 (PCLK_FWH).
 - A5 is connected to B4.
 - A6 is connected to B5.
 - A7 is connected to B6.
 - A8 is connected to B7.
 - A9 is connected to B8.
 - A10 is connected to B9.
 - A11 is connected to B10.
 - A12 is connected to B11.
 - A13 is connected to B12.
 - A14 is connected to B13.
 - A15 is connected to B14.
- Other Connections:**
 - 15,22,24,25,30 PLT_RST1#_B is connected to A2.
 - 15,30 LPC_LFRAME# is connected to A3.
 - 15,19 PCLK_FWH is connected to A4.
 - LPC_LAD3 is connected to A8.
 - LPC_LAD2 is connected to A9.
 - LPC_LAD1 is connected to A10.
 - LPC_LAD0 is connected to A11.
 - EXT_FWH# is connected to A13.
 - LPC_LAD3 is connected to B10.
 - LPC_LAD2 is connected to B11.
 - LPC_LAD1 is connected to B12.
 - LPC_LAD0 is connected to B13.
 - EXT_FWH# is connected to B14.

The diagram also shows the connection of the SA_20080722 component to the U39 chip. The component is connected to the chip's pins A1 through A15 and B1 through B15. The connections are as follows:

- Power and Ground:**
 - 5V_S0 is connected to A1 and B1.
 - 3D3V_S0 is connected to A7 and B7.
 - 3D3V_S0 is connected to A15 and B15.
- Signal Connections:**
 - A2 is connected to B1 (PLT_RST1#_B).
 - A3 is connected to B2 (LPC_LFRAME#).
 - A4 is connected to B3 (PCLK_FWH).
 - A5 is connected to B4.
 - A6 is connected to B5.
 - A7 is connected to B6.
 - A8 is connected to B7.
 - A9 is connected to B8.
 - A10 is connected to B9.
 - A11 is connected to B10.
 - A12 is connected to B11.
 - A13 is connected to B12.
 - A14 is connected to B13.
 - A15 is connected to B14.
- Other Connections:**
 - 15,22,24,25,30 PLT_RST1#_B is connected to A2.
 - 15,30 LPC_LFRAME# is connected to A3.
 - 15,19 PCLK_FWH is connected to A4.
 - LPC_LAD3 is connected to A8.
 - LPC_LAD2 is connected to A9.
 - LPC_LAD1 is connected to A10.
 - LPC_LAD0 is connected to A11.
 - EXT_FWH# is connected to A13.
 - LPC_LAD3 is connected to B10.
 - LPC_LAD2 is connected to B11.
 - LPC_LAD1 is connected to B12.
 - LPC_LAD0 is connected to B13.
 - EXT_FWH# is connected to B14.

The diagram also shows the connection of the SA_20080722 component to the U39 chip. The component is connected to the chip's pins A1 through A15 and B1 through B15. The connections are as follows:

- Power and Ground:**
 - 5V_S0 is connected to A1 and B1.
 - 3D3V_S0 is connected to A7 and B7.
 - 3D3V_S0 is connected to A15 and B15.
- Signal Connections:**
 - A2 is connected to B1 (PLT_RST1#_B).
 - A3 is connected to B2 (LPC_LFRAME#).
 - A4 is connected to B3 (PCLK_FWH).
 - A5 is connected to B4.
 - A6 is connected to B5.
 - A7 is connected to B6.
 - A8 is connected to B7.
 - A9 is connected to B8.
 - A10 is connected to B9.
 - A11 is connected to B10.
 - A12 is connected to B11.
 - A13 is connected to B12.
 - A14 is connected to B13.
 - A15 is connected to B14.
- Other Connections:**
 - 15,22,24,25,30 PLT_RST1#_B is connected to A2.
 - 15,30 LPC_LFRAME# is connected to A3.
 - 15,19 PCLK_FWH is connected to A4.
 - LPC_LAD3 is connected to A8.
 - LPC_LAD2 is connected to A9.
 - LPC_LAD1 is connected to A10.
 - LPC_LAD0 is connected to A11.
 - EXT_FWH# is connected to A13.
 - LPC_LAD3 is connected to B10.
 - LPC_LAD2 is connected to B11.
 - LPC_LAD1 is connected to B12.
 - LPC_LAD0 is connected to B13.
 - EXT_FWH# is connected to B14.

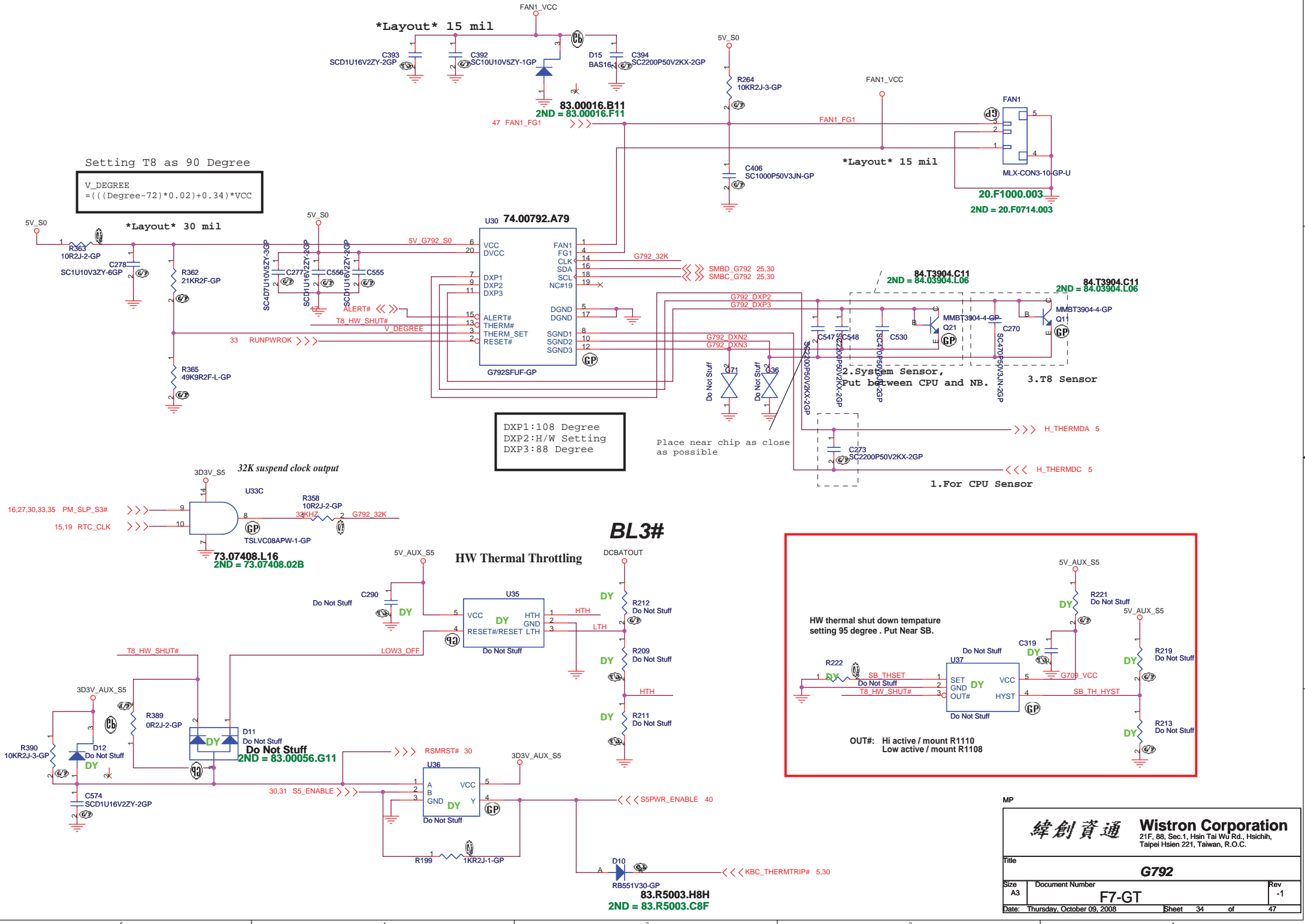


```
37 VRM_PWRGD>>>
```



83.00056.K11

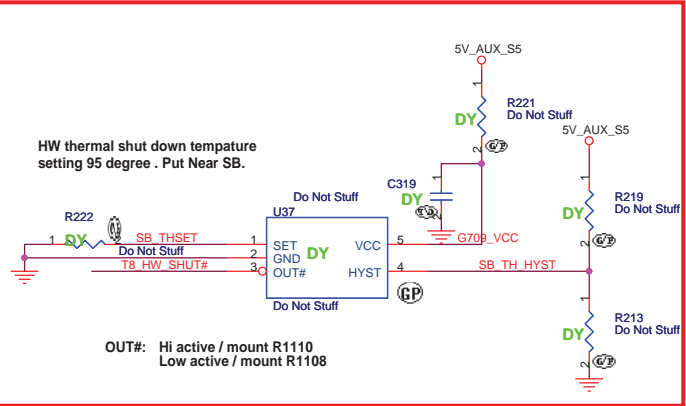
2ND = 83.00056.G11



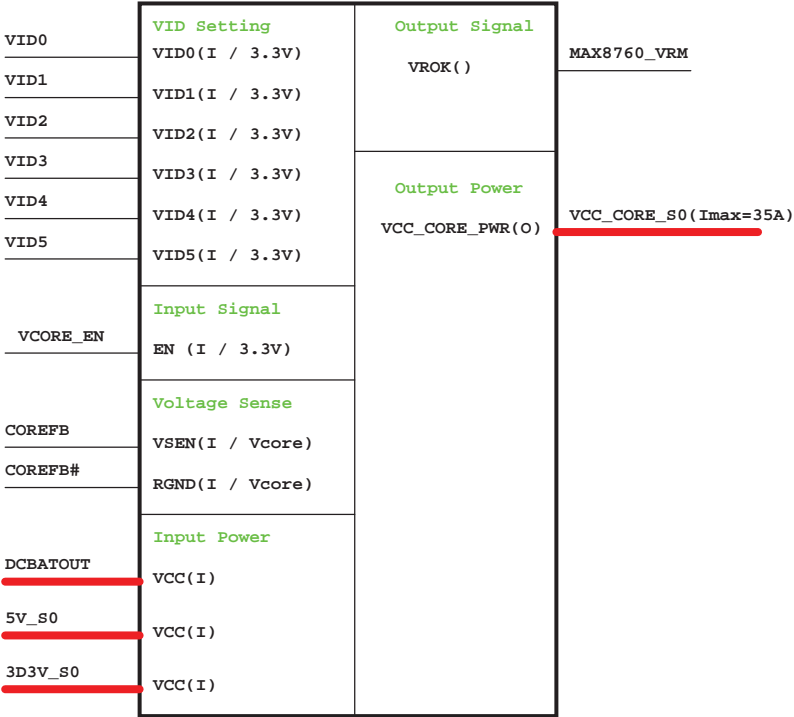
Setting T8 as 90 Degree

$$V_DEGREE = (((Degree - 72) * 0.02) + 0.34) * VCC$$

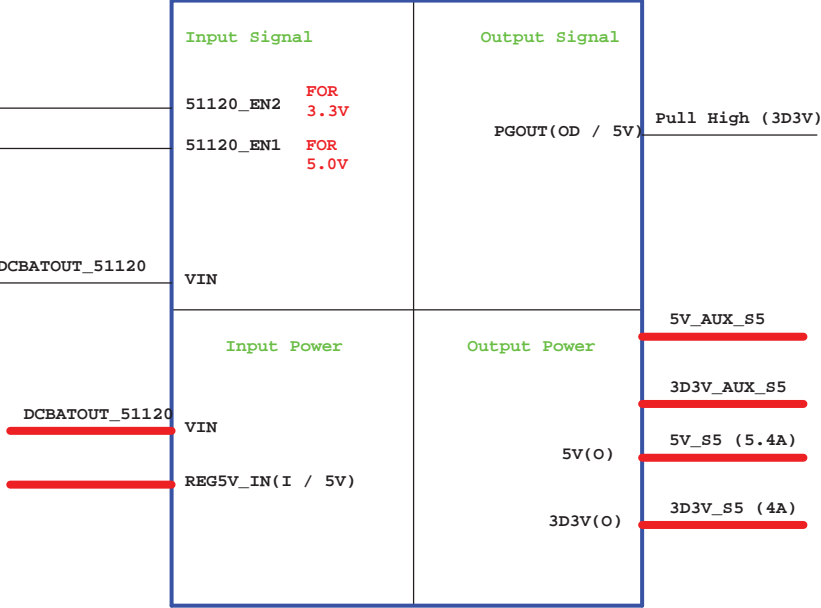
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree



CPU_CORE
ISL6264CRZ



TI TPS51120
3D3V/5V



2D5V_S0



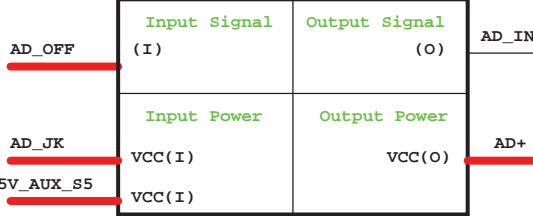
APL5913

1D8V_S5

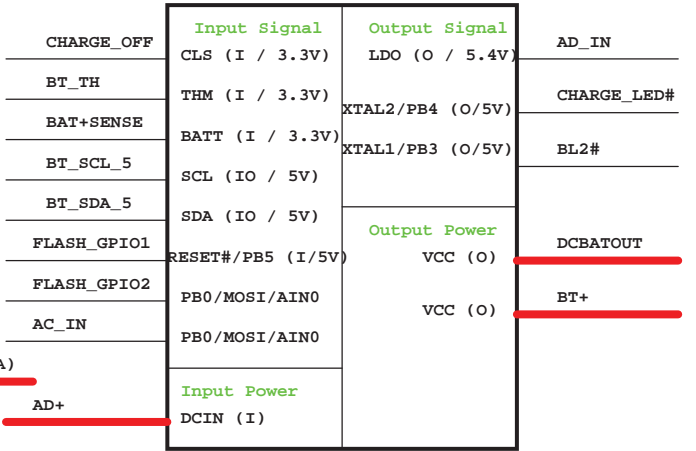


APL5332KAC-TRLGP

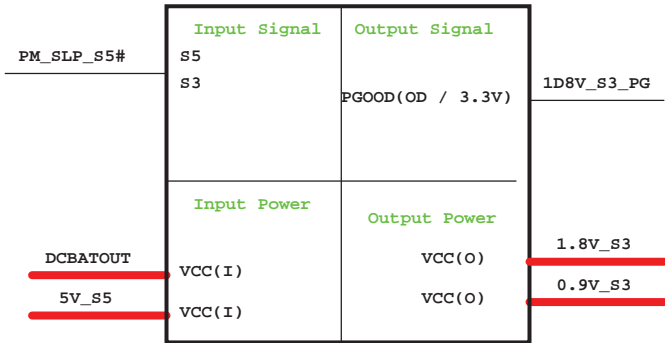
Adapter



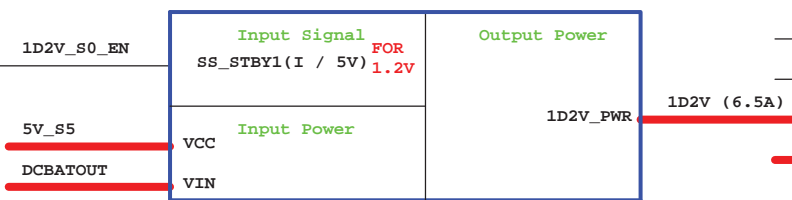
Charger_ISL6255



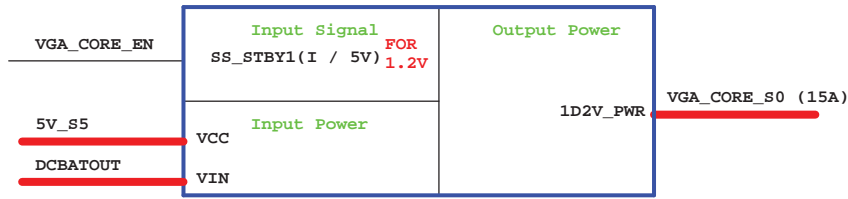
TI TPS51116
1.8V / 0.9V



ISL6268_1D2V

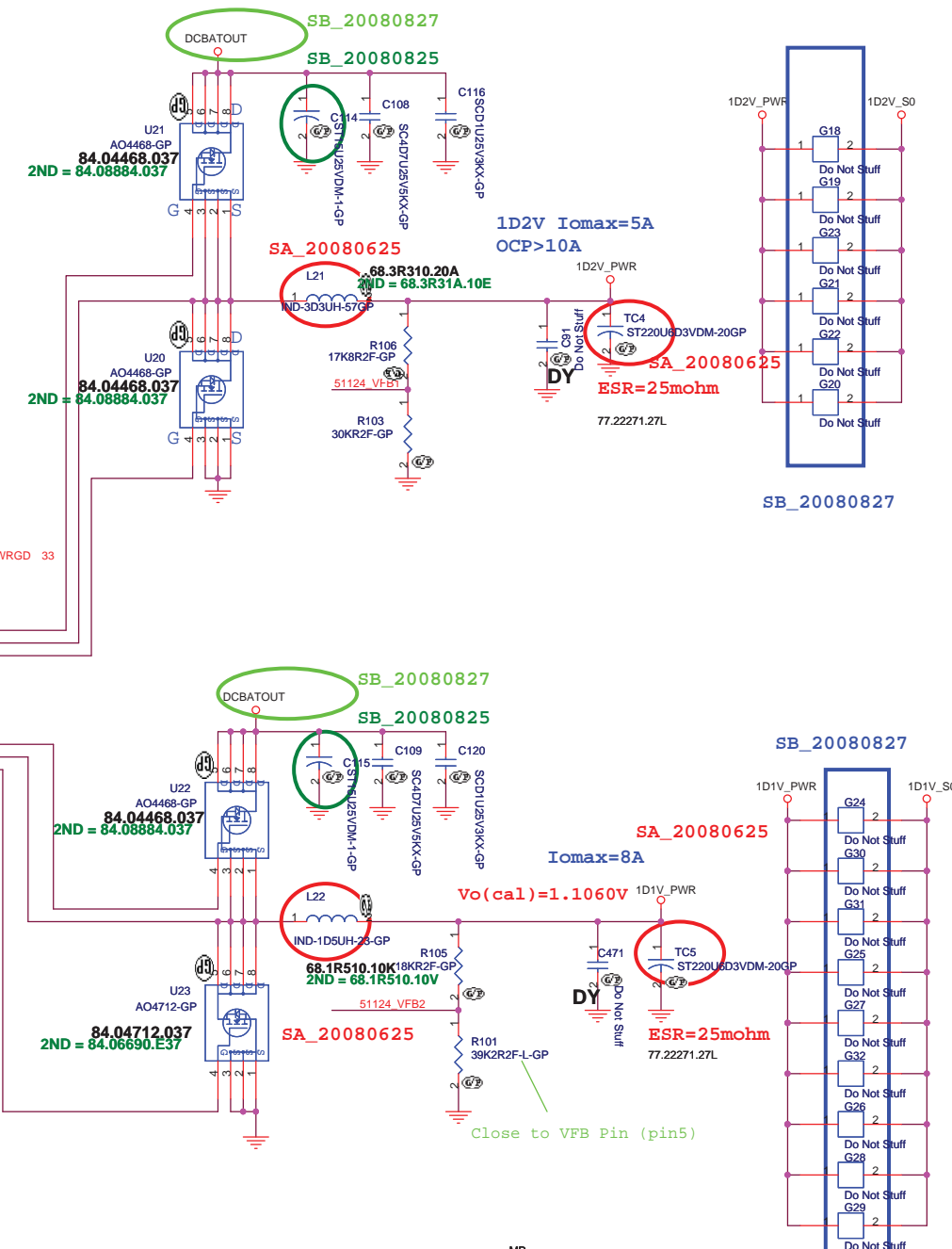
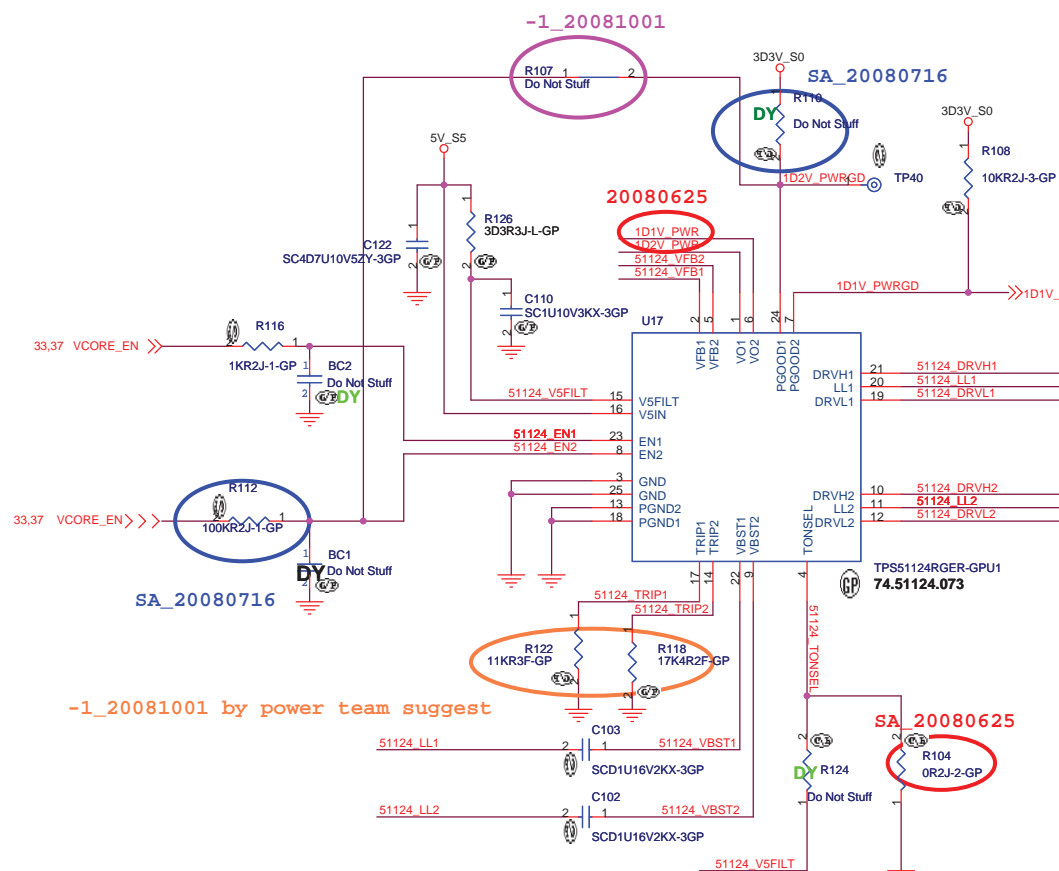


ISL6268_VGA_CORE



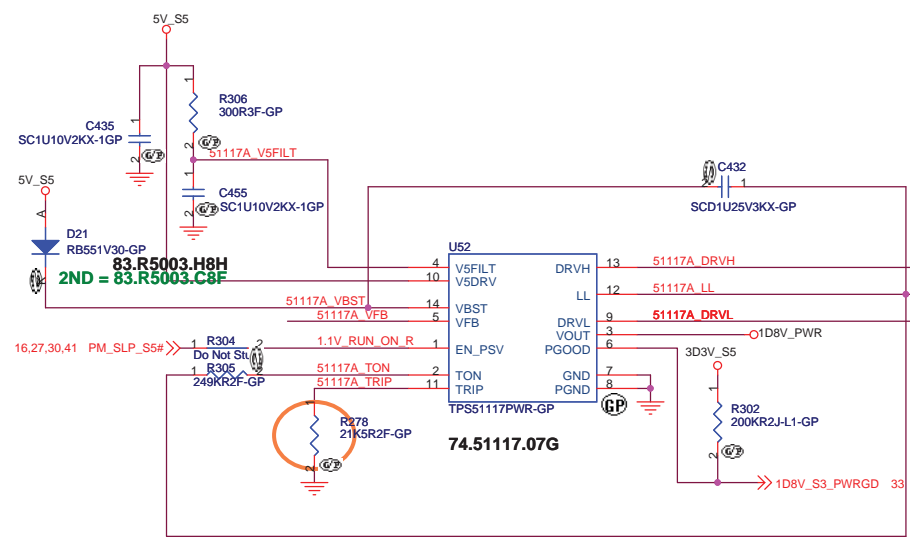
SB 20080827

```
Vtrip(mV)=Rtrip(Kohm)*10(uA)
Iocp=(Vtrip/Rdson)+((1/(2*L*f))*((Vin-Vout)*Vout)/Vin))
```



| | | | |
|--------|----------------------|----------------------|----------------------|
| | GND | OPEN | V5FILT |
| TONSEL | 240k/CH1 300k/CH2 | 300k/CH1 360k/CH2 | 360k/CH1 420k/CH2 |

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode



-1_20081001 by power team suggest

84.04468.037
2ND = 84.08884.037

84.04706.037

Cyntec 10*10*4
DCR=4.2mohm, Irating=16A
Isat=33A

$$V_{out} = 0.75 * (R1 + R2) / R2$$

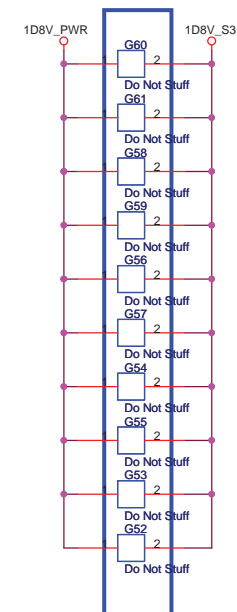
SB_20080827

Vo(cal)=1.8214V

1D8V Iomax=10A
OCP>15A

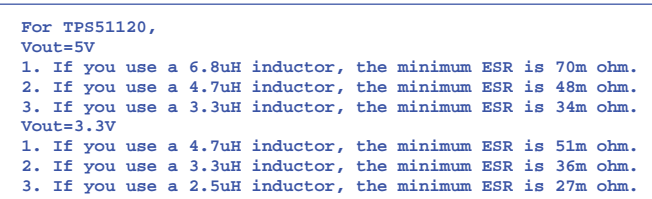
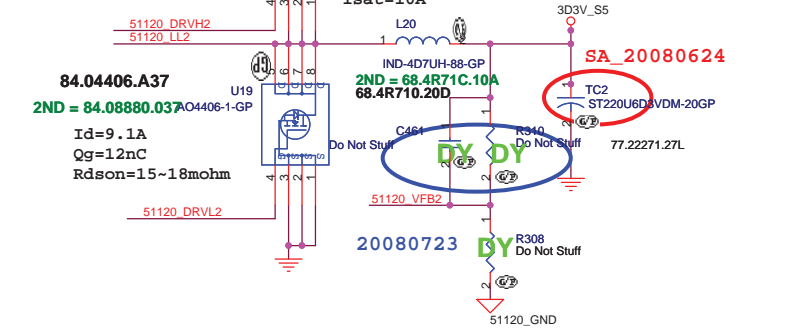
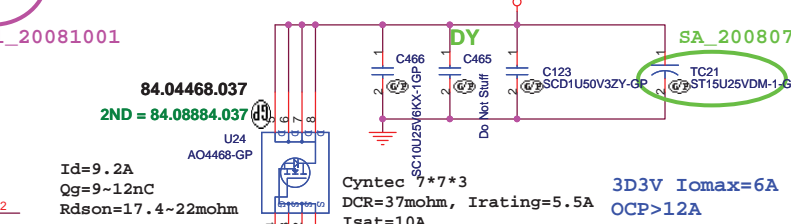
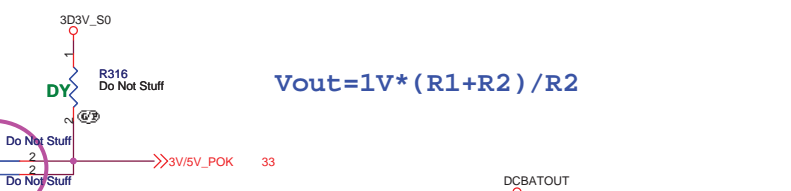
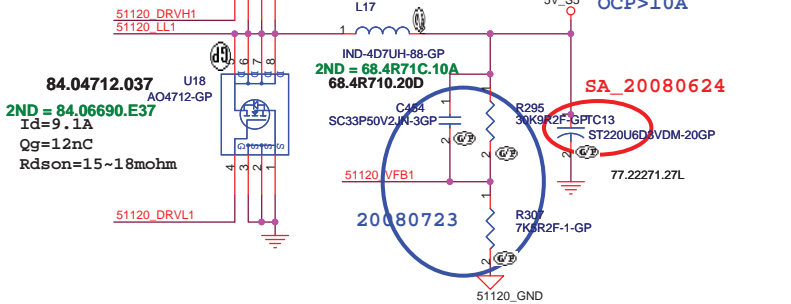
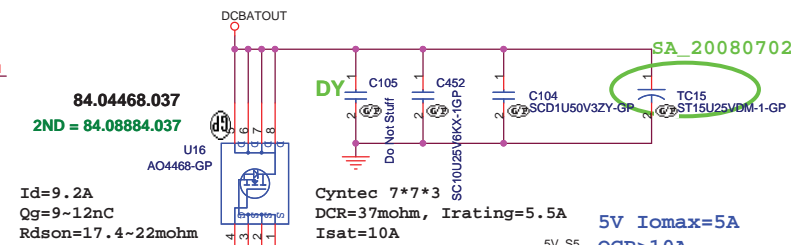
ESR=1.5mohm
2ND = 77.C3371.10L
77.23371.L01


SB_20080827

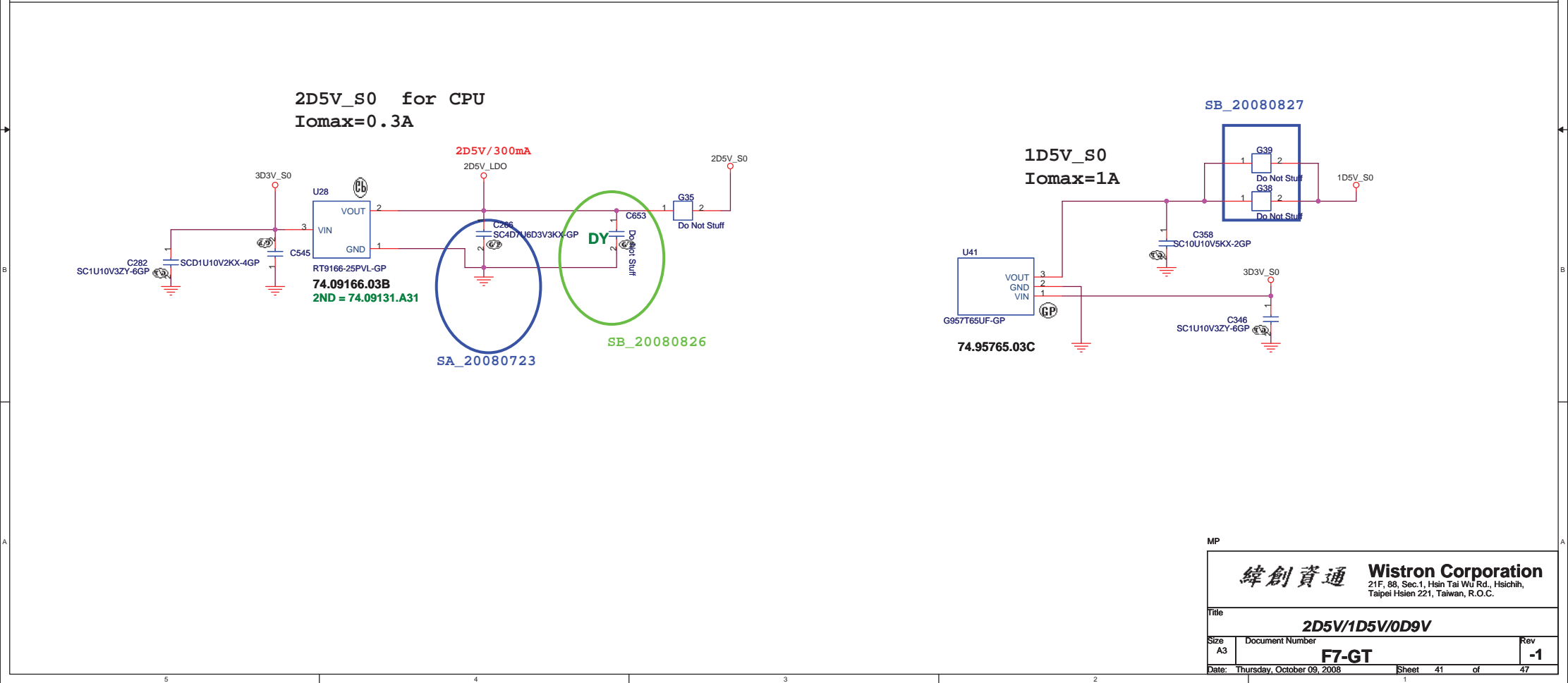
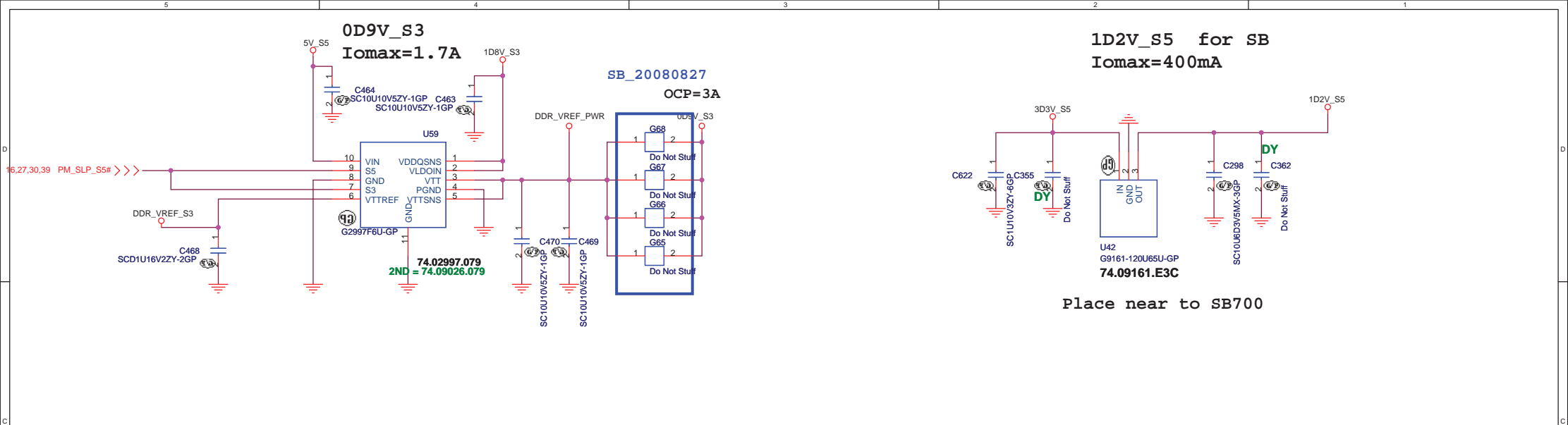


MP

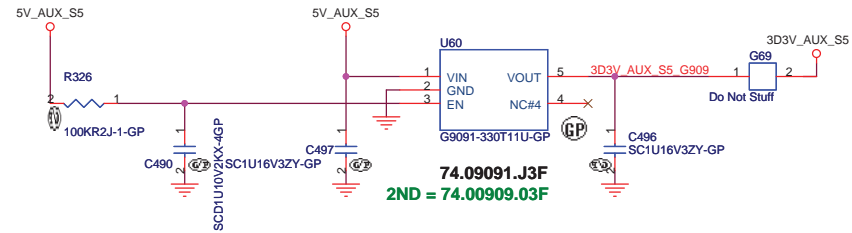
| | |
|---|---------------------------------|
| 緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title 1D8V(TPS5117) | |
| Size A3 | Document Number F7-GT |
| Date: Thursday, October 09, 2008 | Sheet 39 of 47 |
| Rev -1 | |



| | | | |
|---|----------------------------|---|-----------|
| MP | | | |
|  | | Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C. | |
| Title | | | |
| TPS51120 5V 3D3V | | | |
| Size A3 | Document Number | | Rev -1 |
| F7-GT | | | |
| Date: | Thursday, October 09, 2008 | Sheet 40 of | 47 |

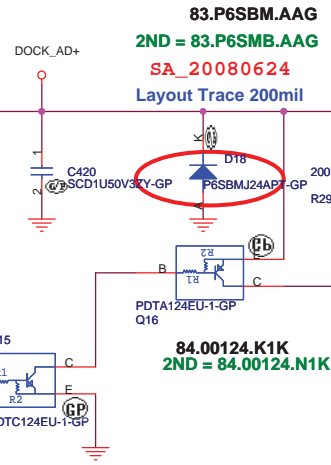
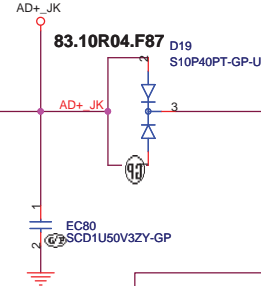
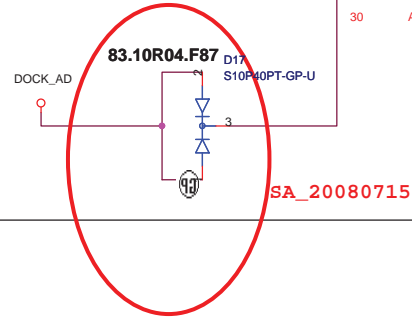
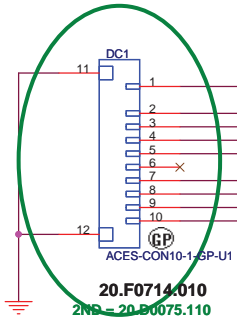


Aux Power 3D3V_AUX_S5



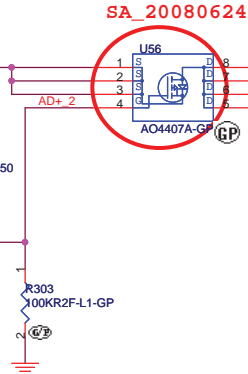
Adaptor in to generate DCBATOUT

SA_20080714

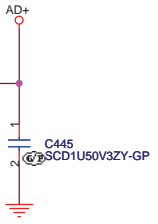


84.00124.K1K
2ND = 84.00124.N1K

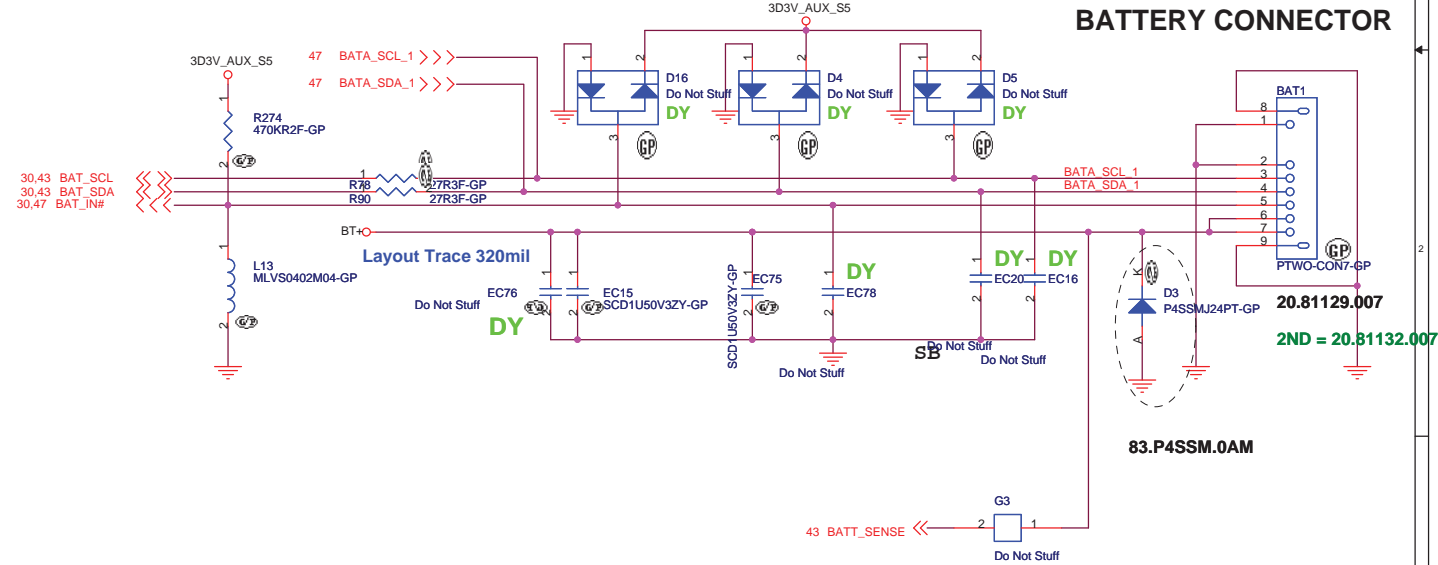
84.00124.H1K
2ND = 84.00124.M1K



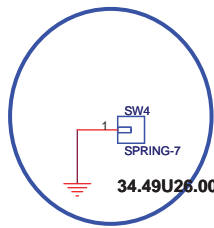
Layout Trace 200mil



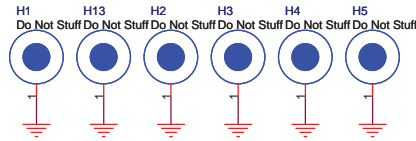
BATTERY CONNECTOR



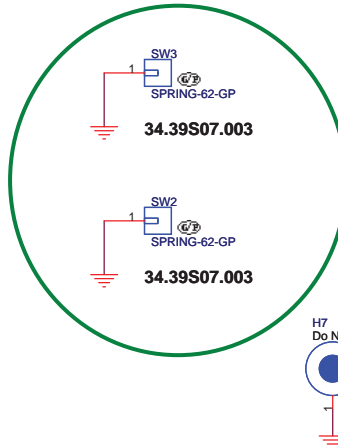
SB_20080827



34.49U26.001

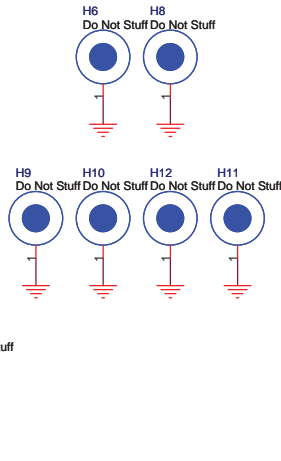


SA_20080725



34.39S07.003

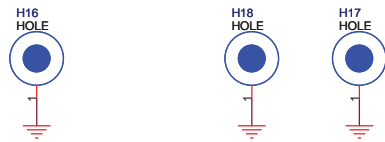
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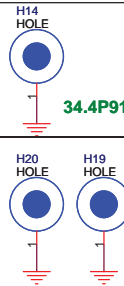
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34.41Q08.011

34.41Q08.011



34.4P910.001



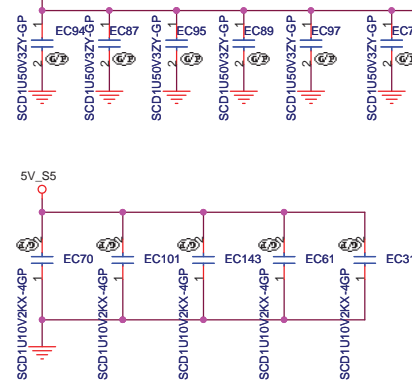
34.4G502.011

34.4G502.011

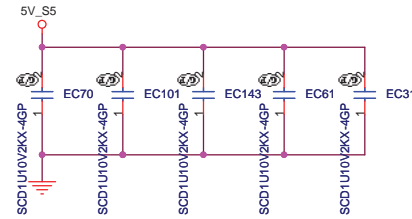


34.41Q08.011

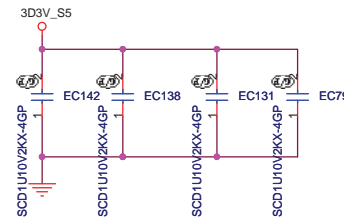
DCBATOUT



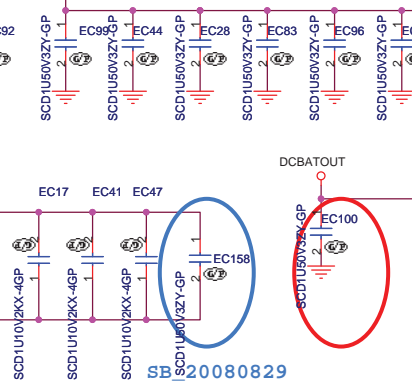
5V_S5



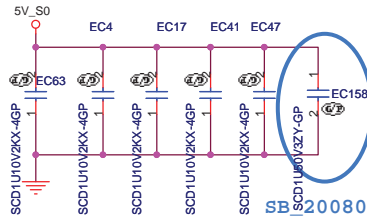
3D3V_S5



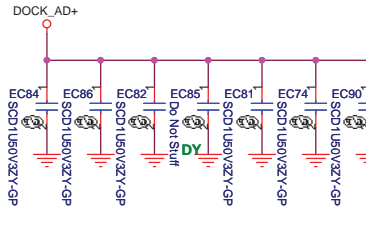
DCBATOUT



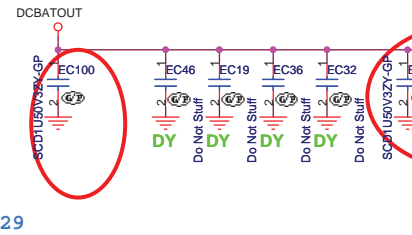
5V_S0



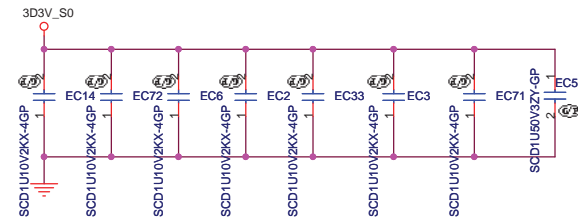
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DCBATOUT



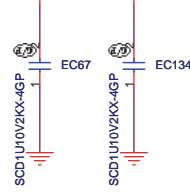
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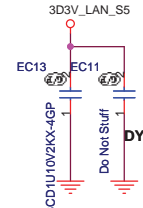
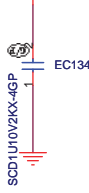
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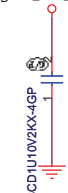
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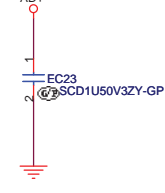
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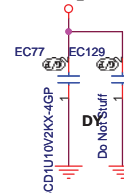
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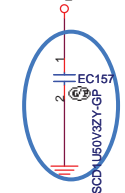
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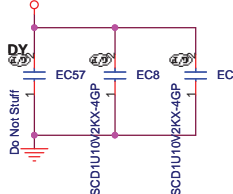


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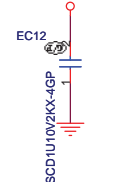


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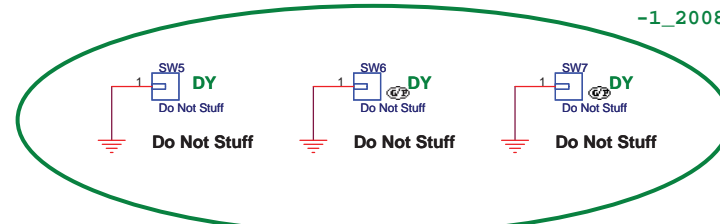
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3D3V_AUX_S5



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